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Open Architecture for Electronic Design & Support Tools

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This is a Small Business Innovative Research Program, Phase I report.

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Under Phase 1 SBIR funding we have outlined an Open Architecture for Testability and Maintainability related tools. We have developed a strawman neutral format for dependency models - the most important and most difficult component of the proposed open architecture, and we have formalized that model using EXPRESS. We have shown in detail how our proposed standards fit synergistically into the framework being developed by the IEEE SCC20 committee, and we have received their provisional approval to proceed under the formal sponsorship of SCC20 (which is an ANSI approved standards developer). Most importantly, we have coordinated with a large group of vendors and users of testability and maintainability related tools, both inside and outside of DOD, and have proven that there is considerable support for such standards.

Open architecture, testability, maintainability concurrent engineering, SCC20, standards, EXPRESS

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Final Report for Period July 1990 - January 1991

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This technical report has been reviewed and is approved for publication.

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OPEN ARCHITECTURE FOR ELECTRONIC DESIGN AND SUPPORT TOOLS

Abstract

Under Phase 1 SBIR funding we have outlined an Open Architecture for Testability and Maintainability related tools. We have developed a strawman neutral format for dependency models - the most important and most difficult component of the proposed open architecture, and we have formalized that model using EXPRESS. We have shown in detail how our proposed standards fit synergistically into the framework being developed by the IEEE SCC20 committee, and we have received their provisional approval to proceed under the formal sponsorship of SCC20 (which is an ANSI approved standards developer). Most importantly, we have coordinated with a large group of vendors and users of testability and maintainability related tools, both inside and outside of DOD, and have proven that there is considerable support for such standards.

These accomplishments exceed our original goals for the Phase 1 effort, and demonstrate that with Phase 2 support, we will certainly succeed in securing an ANSI standard that vendors will support. The standard will, in fact, create an entirely new domain of products which will generate and/or use data compliant with the Open Architecture specification. Without the Open Architecture specification, there would be insufficient potential customers to justify the development of these new products. As part of the Phase 1 effort, we have implemented a prototype of one such tool, which we will develop to completion under Phase 2 funding.

1. Introduction

The Open System Interconnection Reference Model provided a means by which a wide variety of communication equipment could be made to easily interoperate. It provided a means by which communication and network problems could be viewed at a particular level with no concern for how lower levels would implement their capabilities, and with no concern for the details of higher levels. The Open System Interconnection Reference Model has had a tremendous impact on the ease with which diverse equipment can be made to interoperate.

This proposal defines the structure of the equivalent of an OSI model for system design aids, reliability and testability evaluation aids, automatic test vector generation equipment, built in test design aids, diagnostic expert systems, and other similar equipment. The basic concept presented defines the same type of layered interface standards as comprise the OSI model except that the interfaces relate to the diagnosability, testability, and reliability of systems. If fully successful, our Open System Architecture will allow design and diagnosis tools to interoperate as easily as diverse equipment can communicate via the OSI model. The architecture we propose imposes no constraint on how the internals of tools are implemented. The architecture is a set of standard neutral formats for representing the key data structures required for automation of testability analysis, diagnosability analysis, coverage analysis, automated diagnosis, etc. Tools which can input and/or output data in these formats can interoperate.

Computer systems, other electronic systems, and even mechanical systems are becoming increasingly complex. Because of this increasing complexity, it has become essential to develop automated tools to assist a designer. There are many commercial products which

provide aids for the design and validation problem. There are systems which help establish the reliability and testability of a current design. There are products which help generate self testing approaches for systems, and there are a wide range of automatic test equipment. **None of these products interoperate in an integrated manner.** One set of commercial tools cannot be easily used to confirm the results of another because they use different representations of the design, different definitions of values, and different output formats. There is a natural hierarchy of evaluation of reliability, testability, and diagnosability and there are different tools that operate at different levels of that hierarchy, but current tools cannot pass the results of one level of evaluation to the next level of analysis. Our work addresses this critical issue - the interoperability of existing and future design and maintenance tools. Our work to date has proven that our concept is technically feasibility, and that both users and vendors support the idea.

In addition to commercial products, there is a vast amount of current DOD supported research aimed at addressing the above problems. Most ongoing programs are stand-alone tools which help with specific aspects of military system design and life cycle support problems. These tools do not interoperate.

There is some recognition of the need for an Open Architecture for tools related to the testing and maintenance of systems, and some of the work of Standards Coordinating Committee 20 within the IEEE relates to this problem. At his time, however, their work has been limited to the low level aspects of testing. The work which we have done under this task fits perfectly within the overall goals of SCC20, and they have agreed that our work will be done under the AI-ESTATE Committee of SCC20. It is through this committee that our work will become an ANSI standard.

During this Phase 1 SBIR project we have accomplished the following:

a. We have refined the concept of an Open Architecture for testability analysis tools, maintenance aids, logistics support prediction tools, and automated training related tools, and have identified three areas where a standard could be achieved quickly. The three proposed standards are a dependency model, ambiguity group model, and a fault tree model.

b. We have studied the current work items of ongoing ANSI approved committees, and identified the SCC20 as the best formal sponsor for our work. What we propose fits perfectly into their long range goals.

c. We have prepared and presented a briefing to the SCC20, and secured their interim approval to proceed.

d. We have studied and in some cases obtained copies of current commercial tools which are used for testability analysis, and for diagnostic aids.

e. We have developed a strawman formal data model for dependency model data, and have tentatively selected ISO CD 10303-21 as the data encoding standard. Formal data models for ambiguity groups and fault trees should be less difficult to develop.

f. We have generated one relatively complex example dependency model and verified that the dependency data would be representable within our strawman formal data model.

g. We have met with numerous companies which produce testability analysis tools, and which produce real-time diagnosis aids and have secured strong promises of support. We have also met with key leaders of current ANSI Committees and secured their promise of support.

h. We have designed and coded a hypermedia system which shows what a dependency model-based tool could be like. For our system to be widely used, dependency models of systems would need to be available in a standard format.

i. We have developed an example Hypermedia automated Test Requirements Document. The input to this tool consists of ambiguity group data, and fault tree data, plus other ancillary data.

j. We have demonstrated how the above Hypermedia systems can be linked to paperless Hypermedia service manuals. This is usable as a performance aid for technicians, and also could serve as the kernel of a system for automated computer-based training. We have the capability to input existing service manuals (available in paper form only) into the Hypermedia environment using document scanning technology. We can also input manuals available in computer readable form.

2. Need for Standard DOD Data Interchange Formats Related to Testability and Maintainability

Table 1 lists a number of ongoing DOD programs which are developing tool for improving the testability and maintainability of weapons systems. The MATE Program does concern itself with standards but only at the level of the test equipment itself. MATE is not relevant to the higher level issues of concern in Concurrent Engineering. ABET, the last entry in Table 1, will be discussed in more detail in section 4. None of the other programs shown interoperate at all. Each is a stand-alone effort.

Table 2 lists numerous DOD programs which are developing performance aids to help technicians during the diagnosis and repair process. As in the case of the programs listed in table 1, none of the resulting tools will interoperate in any way. There is a need for a standard neutral format for representing the Unit Under Test so that the same input can be used for all of the tools which require the same fundamental information about the Unit Under Test.

DOD tools related to testability and maintainability all use ad-hoc individual formats for their input and output hence one tool cannot be used to validate or refine the results of another.

According to the Institute For Defense Analysis Report P-2300 dated January 1990, some of the most significant problems within DOD related to testability and maintainability analysis are listed below. The quoted sentences are directly from the IDA report.

> "DOD maintenance data collection often originates from verbal inputs with no rigid format requirements." Because of this, it is difficult to make changes to improve the system based on assessments of the current problem areas. The entire system runs "open loop."
>
> "DOD has antiquated, error prone maintenance data collection and feedback capabilities." Without formal standards for the data, accurate results which can be automatically fed into test systems to improve test and repair procedures is not possible.
>
> "DOD lacks centralized data analysis centers focusing on diagnostic accuracy." The concept of a centralized data analysis center would be difficult to implement with data not provided in a consistent format with consistent meaning.

> "DOD maintenance and support functions are paper intensive." Paper manuals are required because there are not adequate "computer-based" manuals.

As described in the IDA report, there is almost complete lack of feedback from the field which could be used to enhance a system's design, production, diagnosis and repair strategies, logistics support, and technician training. The data items shown at the top of figure 1 are all components within the strawman formal data model to be presented later. If our program proceeds, and we are successful in refining and adopting the proposed standard, then all of these data items will be available in a standard format with a standard formal meaning. Not only will data collection now be meaningful but more importantly, that **data can be fed back automatically into the Dependency Model to immediately optimize the test and repair procedures based on the field data.** If automated training systems are based on the standard models, then the training system will also be automatically updated. This point will be elaborated more later in this report after more background has been provided on the model itself and on the types of tools which will likely use the model.

For Concurrent Engineering to be effective, design data must be sharable and usable by design engineers, by test and maintenance system developers, by the logistics support community, by production personnel, and by training and manpower related personnel. This is shown graphically in figure 2. The strawman formal data model for dependency models, for ambiguity group data, and for fault trees contains ancillary data which includes the data items shown on figure 2, plus much more data. More work will certainly be required to expand the current strawman model, but we have made an aggressive start in formalizing and standardizing testability and maintainability related data.

3. Layered Architectures

The development of standards appears to be most effective when individual standards aggregate together into an overall superstructure which relates each individual standard to the intent of the entire system. Layered architectures have been very effective in providing that superstructure and there are several examples of a family of standards which fit within a layered, hierarchical architecture.

The best example of a layered architecture is the International Standards Organization (ISO) Open System Interconnection (OSI) architecture. OSI is composed of seven layers, each of which defines specific services and protocols provided at that level. Figure 3 shows the OSI model. The layers are described below. The key concept is that the functions at one level do not need to know the details of the processes at lower levels or at higher levels.

Layer 1 - Physical Layer	Provides direct mechanical and electrical connection between computer systems or network nodes.
Layer 2 - Data Link Layer	Controls and checks the direct physical connection
Layer 3 - Network Layer	Provides the logical end-to-end connection between control systems when there are intermediaries
Layer 4 - Transport Layer	Controls and checks the logical end-to-end connection
Layer 5 - Session Layer	Provides the logical connection between control programs, or between programs and services
Layer 6 - Presentation Layer	Defines data representations and required data conversion

Layer 7 - Application Layer Provides data services and data management, and may include actual use of the data

Other examples of layered architectures are the National Institute of Standards and Technology Standard Robot Control System Architecture, and the related National Aeronautics and Space Administration NASREM architecture. In these architectures, the tasks of providing intelligent control to a robot is layered, with the lowest layers providing high speed commands for the robot to perform primitive tasks, and at the highest levels, control is long term, and provides task level direction such as move to an object at an initial location, grasp that object, and then move to a destination location and release the object.

We have defined a layered architecture for testability and maintainability analysis. Layered architectures have been successful in other applications, and we believe they are a good match with the technical requirements related to system testability and maintainability analysis. The concept of a layered architecture also matches well with the work of SCC20 described in the following section.

4. IEEE Standards Coordinating Committee 20

Figure 4 summarizes the work of the IEEE Standards Coordinating Committee (SCC)20. The basic concept is a layered architecture.

4.1 SCC20 Reference Model Instrument Layer

The lowest layer is the instrument layer, and specific work is ongoing (IEEEP981) to develop a Test Resource Description Language. This language would be used to define the specific details of the test equipment available. It would define the signals to control the specific test instruments, and would also define the signals need to control the electronic switching matrix used to dynamically connect test equipment to the required test points. The output from the next higher level, plus the RDL description of the test equipment details would be used to generate the proper signals to the test equipment so that the test programs will execute properly.

4.2 SCC20 Reference Model ATE System Layer

The next layer is the ATE System Layer. Everything above this layer defines tests in terms of virtual test equipment, independent of what test equipment with what capabilities are actually available. The Test Equipment Description Language (IEEE P993) will be used to specify what test equipment is actually present and what are its capabilities. (TEDL does not specify how to actually control the test equipment - that is done by RDL).

4.3 SCC20 Reference Model Test Procedure Layer

The Test Procedure Layer gives the actual test program. A major part of the work of the SCC20 is focused on a project called "Ada Based Environment for Test" (ABET) (IEEE1226) and much of the current work of the ABET Committee deals with the Test Procedure Layer. Today, test procedures are typically specified in ATLAS (IEEE 716), and ABET will be the next generation of a Test Definition Language. SCC20 is also working on WAVES - Test Specification Language (IEEE DASS and SCC20-ATPG Committees). WAVES is used to specify specific waveforms used for testing.

4.4 SCC20 Reference Model Test Strategy Layer

The next higher layer is the Test Strategy Layer. This layer specifies in what sequence to execute tests and what to do given specific results from each test. SCC20 has no specific active work items in this area and this is where our work fits into the overall SCC20 architecture. For concurrent engineering, the lower levels of the SCC20 architecture are too low a level to be important. It is the Test Strategy Layer that defines which tests are needed. It is the test strategy layer which uses the data about

Time to Test
Cost to Test
Time to Replace a Part
Cost to Replace a Part
Part probability of failure
Test Reliability
Spares Availability
etc

to generate an optimal test strategy. It is the optimal test strategy which then can be used to compute expected time to repair, overall rate of spares usage, technicians required, cost of maintenance, impact of not having the proper number of technicians available, etc. In our work, we have expanded the Test Strategy Layer into (currently) four sublayers. These four sublayers will be described in more detail later.

4.5 SCC20 Reference Model Product Model Layer

The highest layer in figure 4 is the Product Model Layer. This layer will be based on VHDL (IEEE 1076) to specify the parts themselves. VHDL has three primary levels of detail which cam be thought of as sublayers of the Product Model Layer. The sublayers are the Structural model, Functional model, and Behavioral model. The Behavioral model captures the input-output properties of the modeled component, and it can be used at any level of aggregation of subcomponents. Although VHDL was originally developed for use strictly with semiconductor devices, the behavioral level of VHDL can be used with non-electronic systems as well. The VHDL Behavioral model will provide the primary inputs to the Test Strategy Layer.

5. IAI's Layered Architecture

Figure 5 shows the three layers which IAI has proposed, and how those three layers relate to the Product Model Layer and the Test Procedure Layer of the SCC20 work. The three layers, the dependency model layer, the ambiguity group layer, and the fault tree layer are described briefly below. Figure 6 shows many current testability and maintainability analysis tools which use dependency models, ambiguity groups, and fault trees. None of those tools interoperate even thought they use data which is quite similar. Our work will allow the developers of the tools to write pre and post processors which will convert the standard neutral format into their internal format, and which will convert their internal format back into the neutral format. The benefits of such commonality have been discussed earlier in this final report.

5.1 Dependency Model Layer

Given the detailed model defined in the Product Model Layer, we can generate a dependency model which relates to the tests which are to be performed on the unit under test. A

dependency model specifies what components and what other test results must be good to obtain a good result from any specific test. A dependency model can be thought of as an abstraction of the product model layer. Given a dependency model, testability tools do not need to be concerned with the specific product model in the Product Model Layer. Likewise, the dependency model is a generic concept and the software or techniques used to generate the dependency model are independent of how the model will be used. The analogy to the OSI model is almost perfect. A major goal of our effort under phase 1 funding was to demonstrate the feasibility and utility of a standard for dependency models, and to prove that there will be significant support for this effort from users and vendors of testability and maintainability analysis tools.

A much more detailed discussion of dependency models is presented in section 6 of this final report.

5.2 Ambiguity Groups

The first output of tools which use dependency models to analyze testability and maintainability is ambiguity groups. An ambiguity group means that given the tests listed, it is not always possible to diagnose down to a single part. In some cases a set of parts may be identified as bad, but it is not possible to reduce the uncertainty down to a single component. That set of possible parts is called an ambiguity group. In practice it means that either one part at a time must be replaced and the system re-tested until the bad part is found, or they must be all replaced. Ambiguity groups are caused by two primary problems. First, if there are not enough test points so that individual parts cannot be tested, this causes uncertainty in the result, ie an ambiguity group. Second, if there are feedback loops so that a failure in any of the parts will cause all the parts in the group to look bad because they are not getting the correct inputs from the parts which provide signals to them.

We have defined ambiguity groups as a separate information layer because they are computed from the lower level (dependency model layer) and they are used by the next layer of processing to produce the optimal test strategy in the form of a fault tree.

5.3 Fault Trees

The third layer we propose is the fault tree layer. Fault tree data specifies the optimal sequence of tests for the diagnosis of a specific UUT. It will specify which test to perform, and what operation or test to perform next. Many technician performance aids need a pre-determined fault tree, and other performance aids compute a fault tree in real-time using an internal model of the uut. In the case of design tools which evaluate the testability and maintainability of a proposed design, a fault tree must be computed in order to determine such values as the mean time to diagnose a uut.

5.4 Symptom Library Layer

We are also evaluating the possibility of adding a fourth layer called the symptom library layer. This layer would relate a set of predefined symptoms to the probability that faults exist in specific components of the UUT. The Air Force IMIS (Integrated Maintenance Information System) Program has developed both data structures and algorithms for storing and using symptom data and that work could form the basis of the symptom layer. In many cases, there is no symptom data available. A piece of equipment has been sent to a depot because it has malfunctioned but the nature of the malfunction has not been noted. In this case a symptom layer would not help. On the other hand, in some cases information is available as to how the equipment has malfunctioned and this information should be used to simplify diagnosis.

If we do add the symptom library layer, it would be used to alter the probability of failure data based on symptom information. This would then, in turn, be used to generate new, or alter existing fault trees based on those probabilities of failure.

Symptom information could be derived automatically from the set of failure modes modeled in the dependency model if the dependency model was expanded to include the external symptoms which would result from each of the modeled failure modes. Figure 7 shows all four layers in the proposed architecture.

What we have called the symptom library is similar to what is generally called a fault dictionary but there are differences because a fault dictionary generally uses the results of tests - not failure symptoms in the sense that the information is available before the tests begin. Also, in a conventional fault dictionary approach, the result of the fault dictionary processing is a specific recommendation for part replacement - it is the primary means of diagnosis. In the case of what we have proposed, the symptom dictionary is used only to alter the probability of failure of components before testing begins on the UUT.

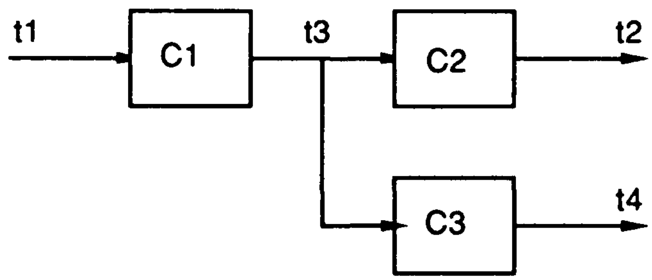
6. Dependency Models

Before proceeding with presentation of the proposed strawman standard for dependency models, we will first present a summary of what dependency models are, and how they are currently used.

6.1 Examples

6.1.1 Example 1 - Very Simple Example

In dependency models, the details of test and response are summarized by giving each test a name, and defining the component of the system tested by that test. The t1, t2, and t3 shown below are tests performed on units C1, C2, and C3. In the figure, we see that t4 depends on component C3 and test t3. Also, test t3 depends on C1 and t1. These are referred to as first order dependencies. By inference, t4 also depends on c1 and t1. This is an example of a higher order dependency. In complex circuits, higher order dependencies can be difficult to determine.



The concept of dependency modeling is very powerful, partly because it can be applied hierarchically. At one level, components can be single integrated circuits, switches, or similar individual components. At the next level, components can be larger aggregates such as a multiplexer, power supply, floating point multiplier circuit, etc. At yet the next level of aggregation, the same exact modelling concept can be used to model subsystems, and assess the testability of the system at that level. The STAT system by DETEX has the capability to automatically take models at one level and aggregate them to the next level.

It should be mentioned that dependency models are not limited to electronic equipment. Dependence-based testability analysis has been used in many domains with equal success.

6.1.2 Example 2. Robot Hand-eye Coordination System

Figure 8 is a system level block diagram of the robot hand-eye coordination system. It is a system which IAI has developed and delivered to the Army Armament, Research, Development, and Engineering Center (ARDEC), Picatinny Arsenal, NJ. The purpose of the system is to demonstrate the capability for a robotic system to catch a freely thrown ball. The system acquires two images from cameras, stores these images in a frame buffer, then converts the two two dimensional images into one three dimensional estimate of the balls position in space, then tracks the object and develops a robot trajectory to intercept the ball, generates a smooth path for the robot to move along, and then sends the smooth path to the robot as a set of move commands.

Figure 9 gives the first order dependency data for the system of figure 8. This data was actually entered into a commercially available dependency-based testability analysis tool (STAT by DETEX). In addition to the first order dependencies, data about the time to run each test, cost to run each test, technicians required, etc was also entered into the tool.

An ambiguity group means that given the tests listed, it is not always possible to diagnose down to a single part. In some cases a set of parts may be identified as bad, but it is not possible to reduce the uncertainty down to a single component. That set of possible parts is called an ambiguity group. In practice it means that either one part at a time must be replaced and the system re-tested until the bad part is found, or they must be all replaced. Ambiguity groups are caused by two primary problems. First, if there are not enough test points so that individual parts cannot be tested, this causes uncertainty in the result, ie an ambiguity group. Second, if there are feedback loops so that a failure in any of the parts will cause all the parts in the group to look bad because they are not getting the correct inputs from the parts which provide signals to them.

Dependency-based tools provide assistance to the designer in identifying ambiguity groups, and in recommending changes to the system to reduce or eliminate groups of greater than one part. The particular tool which we used was STAT by DETEX Systems, Inc but other dependency-based tools have similar outputs. Figures 10 and 11 are STAT outputs for the system of figure 8. The current circuit is very bad because 80 percent of all the parts are in t he same ambiguity group. It would cost $ 5,350 to replace the parts comprising that single ambiguity group. The reason for the ambiguity group is that the frame grabber requires a "GO" signal from the Control module, and the control module depends on the robot to generate a sync signal to it for its timing. This creates one big feedback loop, and the parts in that loop cannot be individually diagnosed because if any one of them fails, the entire loop will stop functioning and there will be no output from any of the modules.

Figures 11 gives summary statistics for the system as it is now designed, and figure 12 gives the optimal test flow sequence for the system. Figure 13 tells the designer where would be the best points to modify the system to break the feedback loop. In this case this would require a test which supplied a separate sync signal to either the frame grabber or to the control module so that the rest of the system could continue to process data. In figure 13, the * indicates the best point to break the feedback loop, at test t12 or test t13.

As an example, we broke the feedback loop at t7 instead of at the recommended t12 or t13. This still left a smaller feedback loop between components 8, 9, and 10. Figure 15 shows the results, and as can be seen there is now still one ambiguity group with three components, and all the rest have only one component each. Figures 16, 17, and 18 give the results of the system with the feedback loop broken at the recommended t13. Now all the ambiguity groups include only one component. Appendix 1 gives the complete input and additional output for example 2.

6.1.3 Example 3 - Detailed circuit for generating signals to force a camera to operate in non-interlaced mode.

Figure 19 is a much more detailed example. The circuit is one developed by IAI and delivered to ARDEC, Picatinny Arsenal, NJ. It is in fact part of the blocks titled Camera 1 and Camera 2 in the system shown in figure 8.

Figures 20 - 23 give STAT output for example 3. Appendix 2 gives the complete input and additional output for the example.

6.1.4 Example 4. Example of Very Detailed Dependency Model

This example was abstracted from "Test Program Sets - A New Approach by Harry H. Dill, Autotestcon 90, San Antonio, TX, Sept. 17-20, 1990.

Consider the simple circuit depicted in Figure 24. Amplifier A1 and its associated resistors, R1, R2, and R3, are configured for a gain of two. Resistor R4 and capacitor C1 form a filter that is designed to have a 30dB cutoff of 1.000 Hz. Current amplifier A2 presents a high impedance to the R4/C1 filter when the output of the circuit is loaded with 50 ohms. TP0, 1, and 2 represent test points, with P1 and J1 representing connector pins. Let us now prepare a detailed dependency model for this circuit.

First, define the failure modes that will require detection. For purposes of illustration, we will define our failures as follows:

Components	Possible Failure Modes
R1, R2, R3, R4, C1	Open Shorted Out of tolerance by more than 20%
A1, A2	Incorrect gain Nonlinear operation

Next, prepare labels for each component and associated failure mode. For the resistors and capacitor, we will append the suffix O to the component name for an open condition (i.e., R1O), S for a shorted condition, and T for an out of tolerance condition. For the amplifiers, we will use a G suffix for gain failures and L for linearity failures. Table 3 lists 19 possible combinations of failure modes and components.

TABLE 3. EXAMPLE UUT LABELS FOR POSSIBLE FAILURE MODES

Resistors			Capacitor	Amplifiers
R1O	R2T	R4S	C10	A1G
R1S	R3O	R4T	C1S	A2G
R1T	R3S		C1T	A1L
R2O	R3T			A2L
R2S	R4O			

O = Open Condition
S = Shorted
T = Out of Tolerance

G = Gain Failure
L = Linearity Failure

TABLE 4. TESTS TO APPLY TO SIMPLE CIRCUIT

Test	Procedure	Dependencies
T101	Apply a 1.0 Vdc signal to input P1. Use a digital multimeter to measure 2.+/-.4 Vdc at TP1.	R10, R1S, R1T, R2O, R2S, R2T, AIG
T102	Apply a 1.0-Vp-p, 100-Hz sine wave to input P1. Use an oscilloscnpe to measure a sine wave of 20+/-0.4Vp-p and dc offset of 0 V at TP1.	T101, A1L
T103	Apply a 1.0-Vdc signal to input P1. Wait 5 seconds and then use a digital multimeter to measure 2.0-0.4 Vdc at TP2.	T101, R40, C1S Note: If A2 + input shortened had been considered a valid failure mode in this example, it would be included with these dependencies
T104	Apply a I.0-Vp-p,1000-Hz sine wave to input P1. Use an oscillcscope to measure a sine wave of 1.4+/- 0.2Vp-p and dc offset of 0 V at TP2.	T102, R40, R45, R4T, C1
T105	Apply a I.0-Vp-p 1,000-Hz sine wave to input P1. Place a 50-ohm load on J1. Use an oscilloscope to measure a sine wave of 1.4+/- 0.2 Vp-p and dc offset of 0 V at J1.	T104. A2G A2L
T106	Use a digital multimeter to measure a resistance of R1 +/- 10% ohms between P1 and TP0.	R10. R1S, R1T
T107	Apply a 1.0-Vdc signal to input P1. Place a 50-ohm load on J1. Wait 5 seconds and then use a digital multimeter to measure 2.0 +/- 0.4 Vdc at JI.	T1O3, A2G

Next, design a series of tests that can detect these failure modes. As we devise each test, we identify which failure modes and tests can be eliminated from consideration if the test passes and identify the set of failure modes and tests that must contain the correct failed component if the test fails. The tests in Table 4, T1O1 through T107, can be performed on the example system.

The dependencies listed in Table 4 for tests T101 through T107 represent the first order dependencies. Higher order dependencies are developed by replacing a dependent test with its associated dependencies. For example, the first order dependencies shown for T105 are T104, A2G, and A2L. This can be represented as:

T105 -> T104, A2G, A2L

Replacing T104 with its dependencies, we have

T105 -> T102, R4O, R4S, R4T, C1O, C1S, C1T, A2G, A2L

Replacing T102 with its dependencies, we have

T105 -> T101, A1L, R4O, R4S, R4T, C1O, C1S, C1T, A2G, A2L

Replacing T101 with its dependencies. we have

T105 -> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, A1L, R4O, R4S, R4T, C1O, C1S, C1T, A2G, A2L.

By a similar analysis, the higher order dependencies for the remaining tests are:

T105 -> T101, A1L, R4O, R4S, R4T, C1O, C1S, C1T, A2G, A2L

Replacing T101 with its dependencies. we have

T105 -> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, A1L, R4O, R4S, R4T, C1O, C1S, C1T, A2G, A2L.

By a similar analysis, the higher order dependencies for the remaining tests are:

T107 --> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, R4O, C1S, A2G.

T104 --> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, A1L R4O, R4S, R4T, C1O, C1S, C1T.

T103 --> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, R4O, C1S.

T102 --> R1O, R1S, R1T, R2O, R2S, R2T, R3O, R3S, R3T, A1G, A1L.

The objective of our testing philosophy is to fault isolate to the smallest set of failure modes possible using a minimum number of tests. To accomplish this objective, we must optimize the sequence in which tests are performed. Information content and test cost are two criteria we can apply to the test sequence decision. In the following illustration, we define information content as the number of failure modes still under consideration in the set of dependencies for a test, and we consider all test times equal. Also, for the illustration, we assume there is a single failure in the UUT.

Using information content as our test selection criteria, we can examine the test sequence that results if capacitor Cl is open. When we begin testing, we have no prior knowledge of what failure modes may exist within the UUT. We want to select the test in our set of tests that provides the most information about the failure modes listed in Table 3.

A review of the higher order dependencies for our set of tests reveals that T105 of Table 4 will check the existence of every failure we are required to detect, and furthermore, no other test in our set of tests can provide this much information; therefore we perform T105 first. (Because C1O is in the dependency set for T105 and C1O is the failure mode on the UUT, T105 will fail.)

In performing T105, we have accomplished two objectives:

(1) We have determined that the UUT is indeed faulty and

(2) We have defined the set of failure modes containing the actual UUT failure.

The set of failure modes defined is the dependency list for T105. Given that all failure modes defined for this UUT are equally likely and that each test in our set of tests has the same cost, the most efficient way to isolate the actual failure mode in the set of failure modes defined by T105 is to select a test that can eliminate half of the T105 dependency elements.

T101 is the best test to do next because 10 of the T101 dependencies are identical to those of T105. If T101 fails, then the intersection of the dependency sets for T101 and T105 must contain the failure mode. If T101 passes, then the T105 dependencies minus the T101 dependencies must contain the failure.

This type of optimization process continues until the fault has been identified.

6.2 Categories of Tests

The examples above described what are called functional tests, but there are other classes of tests which need to be considered in a neutral format which must meet "every" application requirement.

A good description of test categories was described in "System-Level Diagnostics: Simplifying Complexity," by Dr. William R. Simpson of ARINC. His taxonomy is summarized below.

> The simplest form of a test is usually called a FUNCTIONAL TEST The outcome of this test depends on all components and signals that "feed" the test. A good test verifies all components and signals that feed the test, and a bad test implies that one or more of these elements is bad.

A CONDITIONAL TEST is characterized by having more than one set, or list of dependencies. These dependency lists, in turn, depend on (are conditioned by) an event. Such an event may be a scale-setting, a bit selection, mode of operation, etc.

An ASYMMETRIC TEST is a special case of a conditional test in that it uses the dependency list as a function of the test outcome. There are three types of asymmetric tests.

Positive Inference - A test the provides usable information only when the outcome is good. A bad test yields no information.

Negative Inference - A test the provides usable information only when the outcome is bad. A good test yields no information.

Fully Asymmetric - A test that, when the test outcome is good the inference is drawn from one dependency list, and when the output is bad the inference is drawn from a different dependency list.

A LINKED-OUTCOME TEST is a test where the result of one test reduces the dependency relationships for another test.

A SPECIAL TEST is any test which does not fall into any of the above categories. It does not normally monitor the functional health of a system, rather it provides insight into the possible failures within a system.

6.3 Test Data

In addition to dependency data, data is required regarding the tests themselves. The parameters of interest include

Time to perform test
Cost to perform test
Reliability of the test
Test groups
Test groups are groups of tests which, for physical reasons, should be performed together. A typical test group would occur because of the need to set up special equipment . Once that equipment is set up, all relevant tests which could be performed with that equipment should be made at that time.
Sequence groups
Sequence groups are groups of tests which must be performed in a specific order because of the Unit Under Test's requirements relating to the machine state required to run a particular test.
Technician skill level required to run a test
Manpower required to run tests
Test equipment required to run a particular test

6.4 Component Data

Our maintenance tools can also use a priori knowledge about the components of a system. The most important data item is the expected failure rates of the different components. If a given component is much more likely to fail than other components, tests which isolate that component should in general be done first.

Data on part failures from equipment returned from field use, and Retest OK data should also be included.

6.5 Desired Results

Given the required dependency data, data on the tests, and component data , dependency model-based systems can generate the following type of information:

An optimized fault tree
Fault Coverage
Ambiguity group evaluation in terms of numbers and sizes of ambiguity groups, and the specific components in each group
Probability of failure of an ambiguity group
Suggested points to break/control feedback loops to reduce ambiguity groups
Expected false alarm rates
Topological Complexity (TC) Chart
a calculated value that reflects the model's complexity based on the number of tests, dependencies per test, and dependents per test.
Expected average time to diagnose faults
Time to diagnose any specific fault

The optimized fault tree defines the diagnosis sequence which a technician should use to diagnose the UUT. The definition of optimal may be selected by the user by defining the relative weights of each of the test parameters. As and example, the user may specify the relative importance of

cost to test
time to test
usage of critical test equipment
risk associated with making test (to equipment or operator)

With these **importance parameters** specified, the fault tree which is generated will be optimal with respect to the defined parameters and their relative weights. Optimality includes consideration of all of the parameters which the system has data for.

Results such as expected time to diagnose a problem, expected cost to diagnose a problem, and size of ambiguity groups are valuable in predicting life cycle support costs. "What if" analyses can be done by adding test points and observing the changes in these parameters. Certain tests may require technicians with higher levels of training and "what if" tests can be done to evaluate the impact if these technicians are not available, or if those tests are excluded entirely from the test plan.

As field data is available on any UUT type, this data can be entered into the system and used to update the data listed above. This will result in immediate improvements in the optimal test strategy, and improvements in availability estimates, and in maintenance cost estimates, etc.

7. Formal Model

There are two problems associated with developing a formal neutral data interchange format. First a formal data model is required so everyone knows what the data means and how each data item relates to each other data item. Second, a data transfer format must be selected. This second problem is trivial but we mention it for completeness.

7.1 EXPRESS

The approach taken the define the formal data model was to use the International Standards Organization (ISO) Standard called EXPRESS. EXPRESS is an international standard for modeling information. EXPRESS takes the view that a thing (entity) is defined in terms of its attributes, which are represented by other things. A point, for example, might be defined in terms of three real numbers. Names are given to the ingredients which contribute to the definition of a thing. Thus, for a point the three real numbers might be named x, y, and z. A relationship of sorts is established between the thing being defined and the attributes that define it.

Every Entity declared in an EXPRESS schema is considered independent. There is no provision in an entity declaration to closely couple it with another entity from a usage point of view. Rules can be written to effect dependence, but the intent is to make every entity an independent resource.

There are several other formal data modeling approaches but we chose EXPRESS because it is what is being used by the PDES/STEP Committee and we felt that would make our work even more compatible with that much larger program. In addition, NIST has developed an EXPRESS compiler which takes an EXPRESS "program" and complies it into an Oracle database automatically. The NIST system also generates code automatically to populate that database from a data stream encoded using ISO CD 10303 (Product Data Representation and Exchange Clear Text Encoding of the Exchange Structure).

The following pages present the Strawman EXPRESS Model we have generated for Dependency Data. It is intended only as a Strawman, and many improvements and refinements will be required before the model is sufficiently complete to be adopted as a standard. On the other hand, it does crystalize the general concept, clarify what types of data should be included in the model, and it does provide a very concrete place for the AI-ESTATE Committee of SCC20 to begin its formal evaluation of the proposal.

This final report does not provide background on data modeling itself because that would be a several hundred page document in itself. The reader is referred to the many books on the subject, such as "On Conceptual Modelling, " Edited by Michael Brodie, John Mylopoulos, and Joachim Schmidt, Springer-Verlag, 1986. The actual model presented in the following pages is mostly self explanatory. A brief summary of the highlights is presented below.

7.2 EXPRESS model of uut_test

The EXPRESS model of uut_test is given below.

```
ENTITY uut_test;
        --attributes
        test name: string

        --relationships
        has_resources:  SET OF resources;
        has_priorities: priorities;
        has_uut:uut;
END_ENTITY;


ENTITY priorities;
        --attributes
```

```
            time_factor:real;
            cost_factor:real;
            reliability_factor:real;
END_ENTITY;


ENTITY uut;
            --attributes
            uut_name:string;
            explanation:string;
            serial_number:integer;
            reference_docs: SET OF integer;
            uut_input_#: SET [1,#] OF integer;
            uut_output_#: SET [1,#] OF integer;

            --relationship
            has_components: SET [1,#] OF component;
END_ENTITY;


ENTITY resources SUPERTYPE OF equipment, technician;
            --attributes
            has_equipment: SET_OF equipment;
            has_technician: SET_OF technician;
END_ENTITY;


ENTITY equipment SUBTYPE OF resources;
            --attributes
            name:string;
END_ENTITY;


ENTITY technician;
            --attributes
            skill_level:integer;
END_ENTITY;


ENTITY component;
            --attributes
            component_id: integer;

            --relationships
            has_aspect: SET [1,#] OF component_aspect;
            has_replacement_group:  SET OF component_id;
            has_failure_group: SET OF component_id;
END_ENTITY;


ENTITY component_aspect;
            --attributes
            aspect_description: string;
            aspect_id:integer;
```

```
            aspect_inputs: SET [1,#] OF aspect_input;
            aspect_outputs: SET [1,#] OF aspect_output;

            --relationships
            has_component_type: component_type;
            has_conditional_connections: SET [1,#] OF conditional_connect;
END_ENTITY;

ENTITY aspect_input;
            --attributes
            aspect_input:integer;
END_ENTITY;

ENTITY aspect_output;
            --attributes
            aspect_output:integer;
END_ENTITY;

ENTITY component_type;
            --attributes
            component_type: integer;
            component_name:string;
            inventory: integer;
            usage_rate: integer;
            time_to_replace:integer;
            cost_to_replace: integer;
            instructions_to_replace:document_ptr;
END_ENTITY;

ENTITY conditional_connect;
            --relationship
            has_switch_settings: SET OF switch_setting;
            has_good_input_connection/test: SET [1,#] OF input_connection/test;
            has_good_output_connection/test: SET [1,#] OF output_connection/test;
            has_bad_input_connection/test: SET [1,#] OF input_connection/test;
            has_bad_output_connection/test: SET [1,#] OF output_connection/test;
END_ENTITY;

ENTITY switch_setting:
            --attributes
            switch_setting:integer;
            switch_name:string;
END_ENTITY;

ENTITY input_connection/test;
            has_test: test;
            has_input_from_component: component_output
            OR
```

```
                has_input_from_uut_input: uut_input_#
                OR
                has_input_from_uut_output: uut_output_#;
END_ENTITY;


ENTITY output_connection/test;
                has_test: test;
                has_output_to_component: component_input
                OR
                has_output_to_uut_input: uut_input_#
                OR
                has_output_to_uut_output: uut_output_#;
END_ENTITY;


ENTITY test;
                --relationships
                has_test_attributes: test_attributes;
                has_immediate_predecessor: test;
                has_test_group: SET OF test;
                has_predecessors: SET OF test;
END_ENTITY;


ENTITY test_parameters;
                --attributes
                instructions_to_perform_test: pointer_to_text;
                probability_of_false_negative;
                probability_of_false_positive;
                manpower_reqd_to_perform_test: SET [1,#] OF integer;
                test_name:string;
                cost_to_perform_test:integer: integer;
                time_to_perform_test: integer;
                risk: integer;
END_ENTITY;
```

The following sections describe the model, starting with the uut_test. We should make it clear to the reader that the following model is a proposed strawman to begin the process of defining a standard. It is by no means intended as a final model ready for adoption. The strawman should get users and vendors interested in developing a standard, and should convince them that a standard is feasible.

uut_test   uut_test is composed of three sub entities, resources, priorities, and the uut itself

7.2.1 resources

The ENTITY resources identifies the resources available for a particular uut test. Resources include the test equipment and technicians available. Looking at the ENTITY resources, it is composed of two ENTITIES called equipment and technicians. From the formal data

modeling point of view, equipment and technicians are subtypes of resources. In formal data modeling jargon, equipment **is a** resource, and technician **is a** resource. Note that the equipment and technicians required for a particular test are modeled as part of the ENTITY test.

7.2.1.1 equipment

The ENTITY equipment currently consists of only a name which identifies the particular available piece of equipment. This is probably not general enough and more work will be required to allow specification of a capability or class of equipment in addition to a specific unique name for the available equipment.

7.2.1.2 technician

The ENTITY technician contains only one attribute, which is skill_level. This indicates the minimum skill level of the technicians available to perform the uut_test.

7.2.2 priorities

The optimum test strategy depends on weights assigned to parameters called test_factor, cost_factor, and reliability factor. It may be that in a given situation, the time to get a piece of equipment back on line is much more important than the cost of that repair, and in other cases the opposite may be true. The three priority factors allow the user to weigh the importance of time, cost, and reliability.

7.2.3 uut

The uut is modeled with a uut_name, a comment string called explanation, a serial number, reference document numbers, and a list of inputs and outputs, each with a unique number. Most of the definition of uut is contained in the ENTITY component. A uut is composed of a SET OF [1,#] of component. That notation means that a uut must have at least 1 component.

7.2.3.1 component

Each unique component has a unique identification number which identifies that specific component. In dependency modeling, components are broken into aspects. Depending on the exact system, these aspects are viewed as "virtual components" or as component failure modes. A component can have [1,#] OF component_aspect (one or more). Components also have a replacement_group, and a failure group.

7.2.3.1.1 replacement_group

A replacement_group means that when one part of a replacement group is replaced, all the other parts must also be replaced. This is important for diagnosis because it means that there is no reason to diagnose below the level of a replacement group because all the parts must be replaced anyway. A replacement_group is a SET_OF component _id which identifies the group of components included in the replacement group for this particular component.

7.2.3.1.2 failure_group

A failure group means that when a particular part fails, it will have a high probability of causing the failure of the other parts in the failure group. These linked failures result in multiple failures which can be handled in a dependency model based system if they are identified as potential multiple faults.

7.2.3.1.3 component_aspect

Component_aspects have a description, and a unique identifier (called the "dash" number in STAT for example). Component aspects also have sets of inputs and outputs which are each identified by a unique integer, and each component has a component type. The most important part of the formal model for component aspects is the ENTITY conditional_connection. A component is modeled as having a SET [1,#] OF conditional_connections. In dependency modeling, the dependency of a component may be a function of switch settings, initializations, external equipment attached, etc. There may be different dependencies for each case, and these are modeled as conditional_dependencies. A component must have at least one conditional dependency, which means its dependencies are not influenced by other factors.

7.2.3.1.3.1 component_type

Component_type models the characteristics of the particular component independent of this particular component aspect, function, or position of this component in the uut. Component_type models the data generic to the component itself. These include the component name, a unique type number, the number of those parts currently in inventory, the usage rate, time to replace the part, cost to replace the part, and a pointer to the documentation on how to replace the part.

7.2.3.1.3.2 conditional_connection

A conditional_connection can be thought of as a "box" in a dependency model diagram. That box has a set of switch settings which define the particular state of the switch settings, initializations, etc., which give rise to the specific conditional dependency in question. Then the "box" has SET[1,#] OF inputs and SET [1,#] OF outputs. Each such input or output can have a test associated with that connection. The actual interconnection of the "box" to its inputs and outputs is modeled in the ENTITIES good_input_connection/test, good_output_connection/test, bad_input_connection/test, bad_output_connection/test, along with attributes concerning the test itself. The reason why the good and bad distinction is required is that in some cases, tests are asymetric. If a test is good, certain information is obtained, but if the test is bad, a different set of information is obtained. An example, from Dr. Randy Simpson of ARINC, would be an oil pressure light on a car. If the light is on (bad result) it says that there is a fault in the engine, but if the light is off (good result), it gives virtually no information about the engine. The light could be bad, the electrical system could be bad, the oil pressure sensor could be bad, etc. In most cases, however, the dependencies related to a good result and a bad result will be identical.

7.2.3.1.3.2.1 input_connection/test

Input_connection/test has ENTITY test which contains details about the test itself which is associated with that particular input connection. The connection itself is modeled as one of three possibilities - connection to another component_aspect; connection to a uut_input; or connection to a uut_output. These entities specify the exact connection of this particular conditional_connect's inputs to the other component aspects in the model.

7.2.3.1.3.2.2 output_connection/test

Output_connection/test has ENTITY test which contains details about the test itself which is associated with that particular output connection. The connection itself is modeled as one of three possibilities - connection to another component_aspect; connection to a uut_input; or connection to a uut_output. These entities specify the exact connection of this particular conditional_connect's outputs to the other component aspects in the model.

7.2.3.1.3.2.1.1 test

A test is composed of test_parameters which define the particular test and its sequence requirements.

7.2.3.1.3.2.1.1.1 test_parameters

Test parameters consist of ENTITY's which include instructions to perform the test, probability of false negative, probability of false positive, manpower required to perform test, equipment required to perform test, etc.

7.2.3.1.3.2.1.1.2 immediate_predecessor

In many cases, tests must be performed in a specific sequence, generally as a result of the state of the system under test. Test sequences are modeled by defining exactly zero or one specific predecessor tests. Since each test can have a predecessor test, this is sufficient to define the sequence of all tests if that is required.

7.2.3.1.3.2.1.1.3 test_group

It is often the case that tests should be done in groups as a result of physical access, test equipment setup, or other factors. Within a test group, the exact sequence of tests is unspecified but once one of the tests is done, the others should be done before any other tests. Specification of a test group is normally for efficiency purposes.

7.2.3.1.3.2.1.1.4 predecessors

The ENTITY predecessors defines a set of tests which must be done before this test, but the order of those tests is

unimportant except that they all precede the test for which this data applies.

8. Experimental Software

If IAI is successful in developing a standard data model and interchange format for dependency model data, ambiguity group data, and fault tree data, then conforming models for most military and even non-military systems will be developed. This means that a wide range of tools will be able to be developed which use that data. Figure 26 shows some of the tools which might be developed independently by companies. We emphasize that without standards, it would not be economically viable to produce such products because there would not be a large enough market. By developing an open system architecture, we open up the possibility of not one but many commercial products which use or produce conforming data.

We will describe the tools shown on figure 26 in groups.

8.1 Tools to produce better dependency models

Dependency models can be simple and can be generated almost automatically, or they can be very sophisticated and require considerable expertise. Simple models will not have the resolution of a more complex model. Tools which apply artificial intelligence could be developed to generate good models, or improve existing models. These artificial intelligence tools could be rule-based, or they could function using a group technology approach, or they could use a combination of these approaches. In either case their input would be the product model of the uut (plus any existing dependency model) and their result would be an improved dependency model.

Tools which use field data to improve dependency models would be extremely useful and are entirely feasible. These improved models would then be loaded into on-line technician maintenance aids and improved diagnosis would immediately result.

8.2 Tools to produce better physical circuit layouts

Given a dependency model and ambiguity group results, it would be possible to develop tools which would optimize the mechanical layout of a system. As an example, consider a quad logic gate, op amp, or similar component. There are failure modes where all four gates will fail, resulting in four failures. Since most diagnosis tools assume a single failure, the result can be wasted time and unnecessary replacements. If there are several identical gate packages in the circuit, gate selection could be optimized to reduce the probability of false diagnosis due to this problem.

Test points can be physically placed so that groups of tests can be performed together, saving time. A tool to perform this type of optimization could be developed.

8.3 Test Sequence Optimization

Tools could be developed to perform increasingly capable optimization of the test sequence. Such tools would use the dependency model as input and output fault trees. The optimization could use additional data such as historical data for that specific uut (serial number), historical data for that type of uut, or it could perform the optimization faster than other tools, etc.

8.4 Technician Performance Aids, and Training Aids

There are several military systems which use some form of fault tree as a data base to provide on-line aid to a technician performing equipment diagnosis. If there were a standard fault tree format, these tools could interoperate. Tools could be built which provide computer-based training using the fault tree information as a database representing the correct diagnosis strategies.

8.5 Other types of tools

Tools could be developed to generate ATLAS code directly from fault trees. Software to provide on-line TRD's, or for publishing conventional paper TRD's would be more feasible than is the case today because more systems would have conforming representations from which the required data could be easily derived.

The above tools have been discussed to show that there are many opportunities for developing commercial products which exploit the proposed standards. The feasibility of these tools depends on the number of systems to which they could be easily applied, and this greatly increases if a National Standard neutral format could be developed for the required data.

9. IAI's Diagnosis Apprentice

As part of this contract, Intelligent Automation, Incorporated has developed software which we call the Diagnosis Apprentice. This software demonstrates one of the types of tools which will function using the proposed standards.

The Diagnosis Apprentice provides a hypermedia front end to a Test Requirements Document, and also demonstrates many features which would be usable during concurrent engineering activities to improve the testability and maintainability of a system. These features are similar to the features provided by the commercial tool STAT by DETEX Systems, Incorporated. STAT is a dependency model based testability analysis tool which generates a set of paper reports, including a fault tree. With improvements to those algorithms, and with state of the art hardware, our dependency model based system will serve as a real-time technician's aid for use during equipment diagnosis, as well as a tool for performing testability and maintainability analysis during the design of a system. In both of these applications, the user interface will be an intuitive, flexible, hypermedia based interface. Even in the current version of the tool, we have interfaced the diagnosis aid to a computer version of the maintenance manual so that if a particular operation requires reference to the manual, the user will have immediate access to that manual on-line through a hypermedia interface.

9.1 Fault Tree

The Diagnosis Apprentice displays the fault tree for any UUT. See figure 27. The menu visible in the lower right is called the tool set and it can be moved anywhere on the screen, or closed entirely. Once closed, it can always be re-opened using the tool set icon in the upper left corner of the screen. The tool set functions allow the fault tree to be displayed in several different formats (vertical, horizontal, or parallel). Other tool set options are

continuation sheet
test diagram
ATLAS source code
ATLAS flow chart
functional flow
test information
diagnostic flow table
dependency model

9.1.1 Continuation Sheet

A continuation sheet is terminology from a Test Requirements Document (TRD). It refers to explanatory text about a given test. Figure 30 shows an example of a continuation sheet. A continuation sheet refers to a specific test - the test can be determined from a menu which appears if the continuation sheet option is selected from the tool set. If no menu selection is made, the current test is assumed and that continuation sheet is displayed.

9.1.2 Test Diagram

The test diagram shows the interconnection of any required test equipment. Figure 31 is an example of a test diagram. The specific test is selected exactly as in the case of a continuation sheet.

9.1.3 ATLAS Source Code, and ATLAS Flow Chart

Many of the tests called out in the fault tree use automatic test equipment. This automatic test equipment is programmed in a language called ATLAS. The technician may need to see the actual ATLAS code to fully understand what test is being performed and our system will display both a flow chart of the ATLAS code, and the code itself. In both cases, the test of interest is either the current test, or a test selected from a menu (this is identical to the continuation sheet test selection).

9.1.4 Diagnostic Flow Table

Figure 34 shows the Diagnostic Flow Table. This is a small window which can be moved anywhere on the screen, or closed. For any test, it displays the next test or repair step given a good or bad result of the current test. If the **Good** icon is selected, the current test becomes the specified test (in the example on figure 34, the new current test will be T309-1.) If the **Bad** icon is selected, the current test is changed similarly. If either the good or bad test result indicates a repair operation, the correct pages in the repair manual will automatically be displayed. The linkage to the repair manual is discussed later in this report.

9.2 Notebook

For any test, the system designer or the technician can open a notebook and make notes about that particular test. The notes are specific to that particular test. Anything can be entered into the notebook, or things can be copied into the notebook. Figures 35, 36, and 37 all show the notebook opened. The notebook can be moved to any point on the screen, or can be expanded in size with an expansion icon which is barely visible on the upper right corner of the notebook shown in figure 37. Figure 28 shows that test T1010 has been selected by holding down the mouse button with the arrow cursor on the test. This opens a menu in which the notebook is one option, and the notebook can then be selected. The notebook can also be opened from the dependency model diagrams.

9.3 Time to Go and Cost to Go

For any test, the expected time to go to complete the test, and the expected cost to complete the test can be displayed. This option can be opened from the test related menu shown in figure 28, or from the dependency model related menus.

9.4 Dependency Model

Our Diagnosis Apprentice is a dependency model based tool and it is able to display the dependency model of the UUT at any time. Figure 32 shows a dependency model displayed on the screen. The black items are component aspects and they are identified by the I###-# notations inside the box. The tests are identified with T###-# numbers. Because the user interface is hypermedia-based, both the test numbers and the component aspect numbers are active in that selecting those values opens lower level windows or moves the system to other displays.

9.4.1 Ambiguity Group Information

An ambiguity group represents the best diagnosis that can be done with the specified tests and test points. It is often not possible to diagnose down to a single part, and in many cases, a diagnostic procedure will be able to identify the failed part as one of a group of several parts. In this case, either all the parts must be replaced, or a choice must be made, that part replaced, and the system retested. The groups of possibly bad parts is called an ambiguity group. Clearly large ambiguity groups have a major negative impact on the cost and time to repair a faulty system. For any part, the Diagnosis Apprentice will display the ambiguity group containing that part. It will often but not always consist of one part. The top window in figure 30 shows an ambiguity group for part I319 -1. On the upper left of the window, an icon allows display of all the tests which test that part. Selecting that test will result in the correct point in the fault tree which contains the selected test to be displayed.

In addition to the ambiguity group, the window on the top of figure 33 also indicates the cost to replace all the parts in the ambiguity group, and the time to replace all the parts in the ambiguity group.

The designer can use the Diagnosis Apprentice to perform "what if" analysis to determine the benefits from adding additional test points, to breaking feedback loops, etc. This is one of the primary uses of existing dependency model based tools, and our system will make that capability easier to use, and the standards we are working toward will make the produce all the more cost effective and practical to use.

9.4.2 Test Cross Reference

As shown in the window in the lower right of figure 33, the system will also display the number and size of ambiguity groups which are in the dependency list of a given test. Selecting the test from the window specifically identifies the groups and selecting the ambiguity group icon displays the ambiguity group details as described above.

9.5 Additional Features

The current version of the Diagnosis Apprentice was coded as an example of the type of system which could be implemented. With follow-on funding we will be able to implement all of the features in current systems such as STAT and STAMP for use during design, and all of the features of POINTER or GADDS for use as a real-time technician's aid in performing diagnosis and repair.

9.6 Interface to Maintenance Manuals

Figures 35 to 41 show example screen shots from the automated maintenance manual which IAI has interfaced to the Diagnosis Apprentice so that when specific instructions are required by the technician, they will be immediately available without having to find and use paper manuals. It should be noted that the software which implements these functions was developed under funding from the U.S. Department of Education, and from the U.S. Naval

Air System Command. Its adaptation for use with the Diagnosis Apprentice was done as part of the subject SBIR contract.

Some of the features of the user interface are described briefly below.

9.6.1 Outline

Our manual display system provides several tools to allow the user to move easily and naturally through the document so that they will always know where they are, and how to get to any specific point. This is an important feature because research has shown that one problem with hypermedia systems is that users "get lost" in the sense that they are not sure where they are or how to get back to any previous point. As shown in figure 35, a table of contents is visible on the upper left of the screen. This field is scrollable, and also can be expanded to full screen size by clicking on the expand icon in the upper right of the table of contents field. The expanded image is still scrollable. Clicking on any point in the table of contents causes the document display to move to the selected point in the text.

9.6.2 Main Text Window

The main text window displays the text on the current page of the maintenance manual. The field is scrollable in the event that not all the text is visible at one time however this will rarely occur because the import tools which transform the text into hypermedia form divide the text in the paper manual into multiple pages for display on the screen. The actual page number of the material in the paper document is displayed but several pages of screen display may equal one paper page. This format was selected after extensive research into how much information should be displayed on a computer screen at one time.

It should be noted that because we do not want a user to be able to alter any of the primary document, all the text visible in the main window is **locked** text and cannot be changed. Notes can be taken, and supplemental text or graphics can be added by an authorized user as will be described later, but the formal document cannot be modified. In Macintosh software, locked text cannot be selected. Since many of the features of the Diagnosis Apprentice require selection of text in the main window (locked text), we had to circumvent and/or modify several aspects of Supercard.

9.6.3 Figures

As shown in figures 35, 36, and 37, figures associated with the text on a given page is displayed on the upper right of the screen. The figure will automatically change as the text changes so that the correct figure will always be visible on the screen. The figure can be expanded to full screen size by clicking on the expand icon. A small part of the icon is barely visible on the upper right of figure 35. Clicking on the icon again returns the figure to its small size. When expanded, forward and backward arrows are also visible which can be used to "leaf" through the figures, either forward or backward.

9.6.4 Notebook

The user can make notes in a notebook associated with any specific test. The notebook window is scrollable, and is also expandable to fill the entire right half of the screen. The expand (and contract) icon is barely visible in figure 37. Arbitrary notes can be typed into the notebook, or they can be copied into the notebook from any other text. The steps to mark and then copy text are similar to the normal way to mark and copy text in any of the Apple Macintosh word processing packages. Clicking once on a word selects the word. Clicking twice on a word selects the entire sentence. Clicking on any word and then holding down the

shift key and clicking on any other word selects all the text between the two words. The edit icon at the top of the notebook window contains the usual copy and paste services.

9.6.5 Glossary

There is an on-line glossary which will give the definition of any selected word which is contained in the glossary. The glossary is shown on the top of figure 36, where the definition of the acronym MGM is currently displayed in the glossary window. Once a definition is displayed, clicking on the page icon will cause the text where that term was first used in the entire document to be displayed in the main text window. The concept is that the place where a term is first used is the place where it is most completely defined. Clicking again on the page icon causes a box to be drawn around that first occurrence of the word on the page currently displayed on the screen. The glossary is scrollable, and can be closed by selecting the close icon. The glossary window is not expandable.

9.6.6 Speech

A speech synthesizer will verbalize any selected text when the speech icon is selected. The text is selected exactly as text was selected to be copied into the notebook. This was described in section 9.6.4 above. Any text in the main text window, in the glossary, or in the figure captions can be selected.

9.6.7 Import Tools

Some of the tools provided for importing supplementary material are shown on figure 37 and are described below. There are also a set of tools for importing existing maintenance manuals, but those details are beyond the scope of this report. We would be pleased to provide additional details on request.

9.6.7.1 Linking of Video Sequences from a video disk

At any point in the text, a section from a video disk can be linked into the text. Figure 37 shows the set of tools which can be used for importing supplementary materials, as described in section 9.6.7. Selecting the video disk player controller and the video link editor menu items causes the windows shown in figure 38 to be displayed. Using these fields, the video disk can be controlled, and using the linking tools, the correct place in the text can be linked to that point on the video disk. During use, if there is a supplemental video section associated with a particular section of text, an icon will appear at the bottom of the screen. If the user selects this icon, the video player will automatically position to the correct point, and play the sequence as defined by the links. The video link editor and the video disk controller windows can be moved anywhere on the screen, and can be closed by clicking on the close box in their upper left corner.

9.6.7.2 Add Explanation, Import Pictures

Supplemental material can be added to an existing manual without changing the basic document which has been approved for use. Our system has tools for linking both supplemental graphics or supplemental text. In these cases, icons will appear at the bottom of the screen to indicate that there is supplemental material present. That material can be displayed by clicking on the appropriate icon. Graphics can be imported by scanning an existing picture, or a video camera can be used to capture an actual image, which will be linked into the document exactly as it would if the image had been scanned.

9.6.7.3 Add Questions

One of our goals in developing the automated maintenance manual described above is to be able to use the system in a computer-based training system. As shown on figure 37, some of the tools which we created allow questions to be included with the manual. If there have been questions added, a "question" icon will appear at the bottom of the screen. Room is provided for the "student" to answer the question, and aids are also provided to help the student answer the question. Since these capabilities are not directly relevant to the subject work, we will not go into detail as to these functions and services.

9.6.8 Hierarchical Figures

Figures 39, 40, and 41 show the types of links that have been implemented between figures and the instructions related to those figures, and between figures and the subparts of those figures. Figure 39 shows a figure and a list of subcomponents of that figure. When one of the subcomponents is selected with the mouse, a large red arrow points to the particular subpart. Figure 40 shows instructions for performing a repair operation on the displayed part. When the specific instruction is selected, arrows are drawn to the parts. Then selecting the parts identified by the arrow causes expanded views of the parts to be drawn in a separate, movable window. Forward and backward arrows can be used to view all of the subcomponents if that is desired.

10. Major Example

ARINC has provided IAI with the dependency models used for testability analysis and for on-line diagnosis of the A2 and A3 shop replacable assemblies for the high voltage power supply from the AV-8B heads-up display. The A3 dependency file contains 33 tests and 120 components and supports fault isolation to 42 groups of 1 or more components. The A2 dependency file contains 23 tests and 64 components and supports fault isolation to 32 groups of 1 or more components. The tool for which the dependency model was prepared was POINTER, developed and marketed by ARINC.

We have taken the dependency model provided by ARINC and converted it manually to the formal data model detailed in section 8 of this final report. There were no problems associated with the conversion although it was not the most conclusive test of the adequacy of the neutral format because the particular dependency models (for the A2 and A3 shop replacable units) had no conditional dependencies or asymmetries.

Then, to demonstrate that the data could then be transferred from the neutral format to the internal format of a different commercial tool, we manually converted the data from the neutral format into the format of STAT by DETEX Systems, Incorporated. Again, the conversion was simple because the dependency model was quite simple (even though it was for an actual component in systems currently in use by the Air Force).

The models are quite verbose and are not included in this final report but they will be provided on request. Appendix 3 is the STAMP input data for the simpler of the two power supplies used in this experiment - the HVA2 High Voltage Power Supply A2 Model for the AV-8B heads-up display.

11. Outside Support

As part of our Phase 1 SBIR contract, we have spoken to many users and vendors of tools for testability and maintainability analysis. All of the people we have spoken to were supportive of our work. We have received support from:

Bradford Smith, Chairman of STEP (International part of PDES and an important part of the CALS Program)

Ralph DePaul, President of DETEX Systems, Incorporated

Randy Simpson, Designed and Implementor of STAMP, and POINTER

Robert Rolfe of the Institute for Defense Analyses, key participant in ABET

Leslie Orlidge, Chariman of the AI-ESTATE Committee of SCC-20

John Bloodgood, Technical Advisory Group (TAG) Chairman of TC 184/SC 1 - *NC of Machines* and SC 5 - *Systems Integration and Communications*. Acting TAG Chairman of TC 184/SC 2 - *Industrial Robots:* Current Chairman of IEC/TC 44 *Electrical Equipment of Industrial Machines*

We have also received support from numerous DOD representatives including

Dr. Bob Hillman of Rome Laboratories
Christine Fisher, Office of the Secretary of Defense (P&L) SS&T

We have also received support from Narayan Ramachandran of TYX Corporation, and Douglas Van der Heide of Van der Heide, Inc., TYX Corporation produces a tool named PAWS. DETEX Systems, Incorporated and TYX Corporation have developed an exchange format which allows the output of STAT (DETEX) to be used without change as the input to PAWS (TYX). The exchange format has helped both companies, and is an example of what could be achieved with a National standard. Van der Heide, Incorporated produces a tool called TAD (TRD and ATLAS Development).

No one we have talked to has been negative.

We made a 20 minute presentation to the full IEEE SCC20 committee at its plenary meeting, and submitted a formal PAR (Project Authorization Request). Figure 42 shows the cover page for the presentation, and figure 43 is the actual PAR. We were given provisional approval to proceed with development under the formal sponsorship of IEEE SCC20 - an ANSI approved standards writing body. There were over 150 people at the SCC20 meeting, and I received many very positive comments. I had made 50 copies of the presentation, and gave them out only when I was asked for a copy. I ran out of copies and more had to be copied at the meeting.

MAJOR DOD PROGRAMS RELATED TO WEAPON SYSTEM TESTABILITY AND MAINTAINABILITY

(From 1987 report to AMC by IAI - may now be obsolete)

Integrated Diagnostics Support System (IDSS)

Modular Automatic Test Equipment (MATE)

Reliability and Maintainability Factors in Computer Aided Design
(RAMCAD)

"SMART" Bit Techniques

Tester Independent Support Software System (TISSS)

Test Engineers Assistant (TEA)

Computer Aided Design/ Built In Test (CAD-BIT)

Atlas Test Support Environment (ATSE)

Avionics Integrity Program (AVIP)

Ada-Based Environment for Test (ABET)

Table 1. DOD Testability and Maintainability Analysis Tools and Programs

PERFORMANCE AIDS

Smart Maintenance Trainer

Integrated Maintenance Information System (IMIS)

Computer-Based Aid for Troubleshooting (CBAT)

Predictive Aircraft Maintenance System (PAMS)

Intelligent Maintenance Training System

Versatile Maintenance Expert System

Consolidated Automated Support System (CASS)

Electronic Information Delivery System (EIDS)

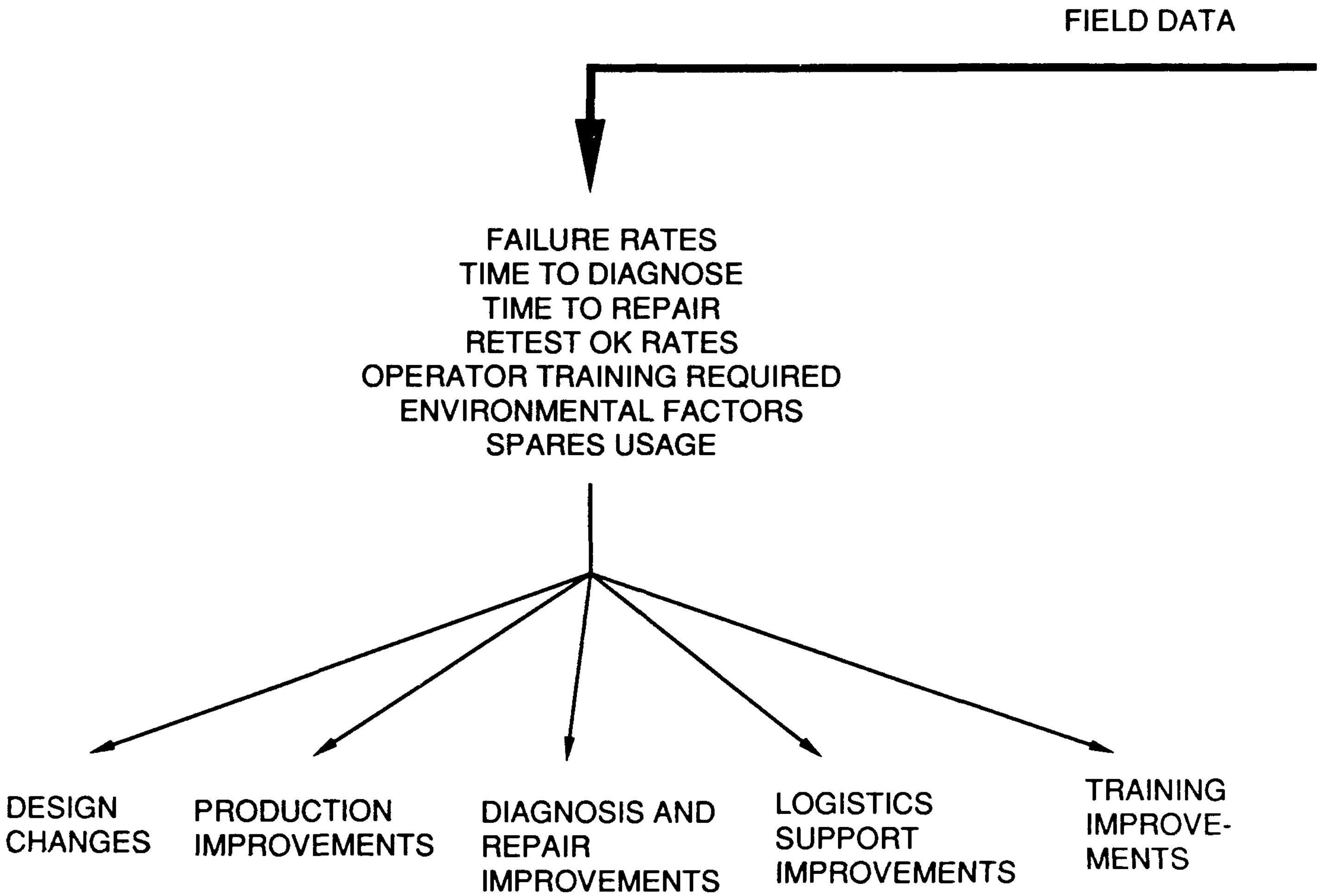
Intermediate Forward Test Equipment (IFTE)

Miniaturized Electronic Information Delivery System (MEIDS)

Personal Electronics Aid For Maintenance (PEAM)

Integrated Maintenance Information System (IMIS)

Table 2. DOD Maintenance Technician Performance Aids

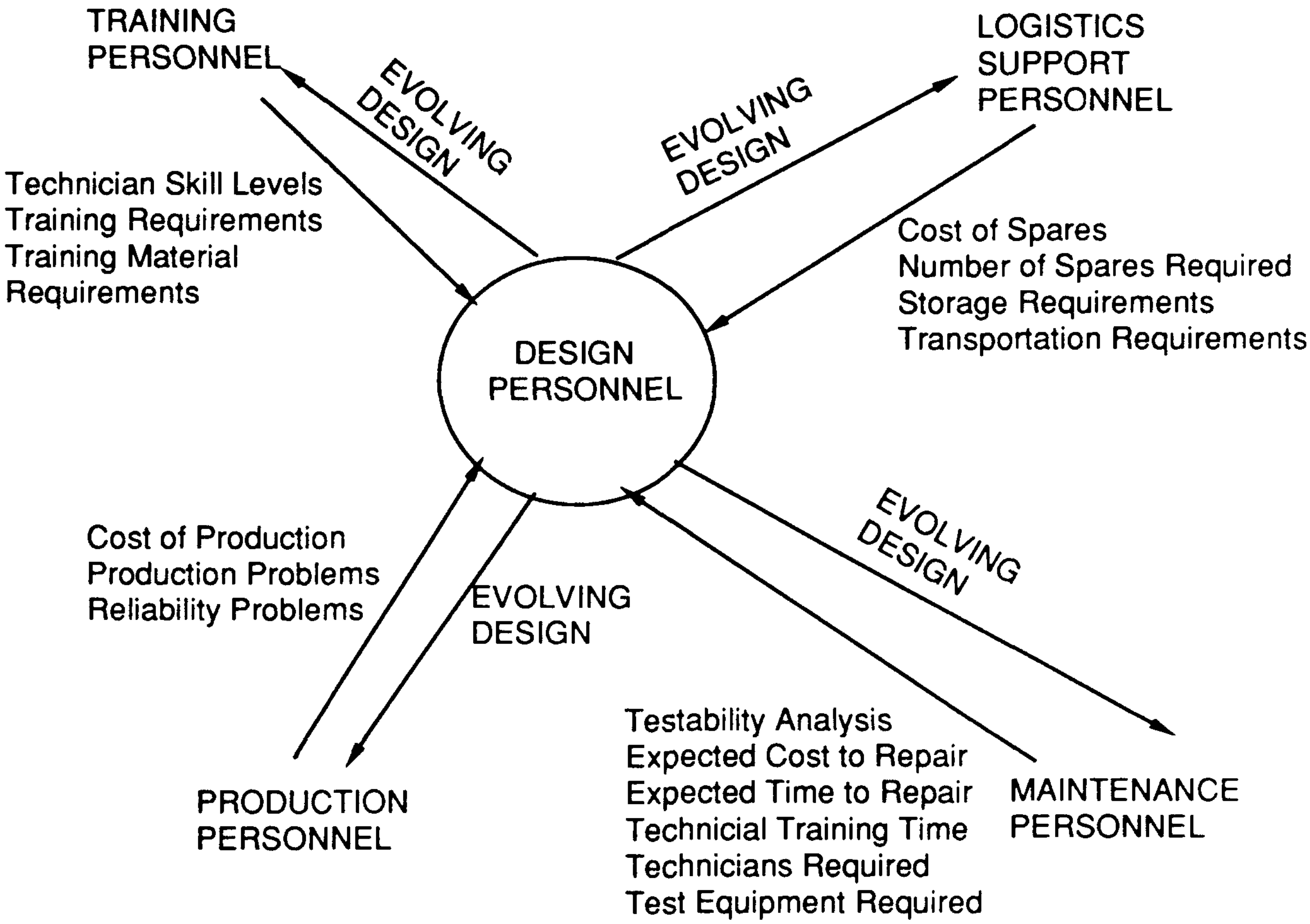


ACCURATE AND EFFECTIVE USE OF EXPERIENTIAL DATA REQUIRES FORMAL DEFINITIONS OF THE DATA, AND STANDARD INTERCHANGE FORMATS.

THE DATA MUST BE COMPATIBLE WITH THE TOOLS THAT USE THE DATA

Figure 1. Use of Field Data

CONCURRENT ENGINEERING REQUIRES INFORMATION TO BE SHARED



FOR CONCURRENT ENGINEERING TO WORK, DATA MUST BE SHARABLE OVER A WIDE RANGE OF TOOLS

DESIGN TOOLS
TESTABILITY AND MAINTAINABILITY RELATED TOOLS
LOGISTIC SUPPORT TOOLS
PROCESS PLANNING AND PROCESS CONTROL TOOLS

DATA EXCHANGE STANDARDS ARE ESSENTIAL

Figure 2. Shared Data

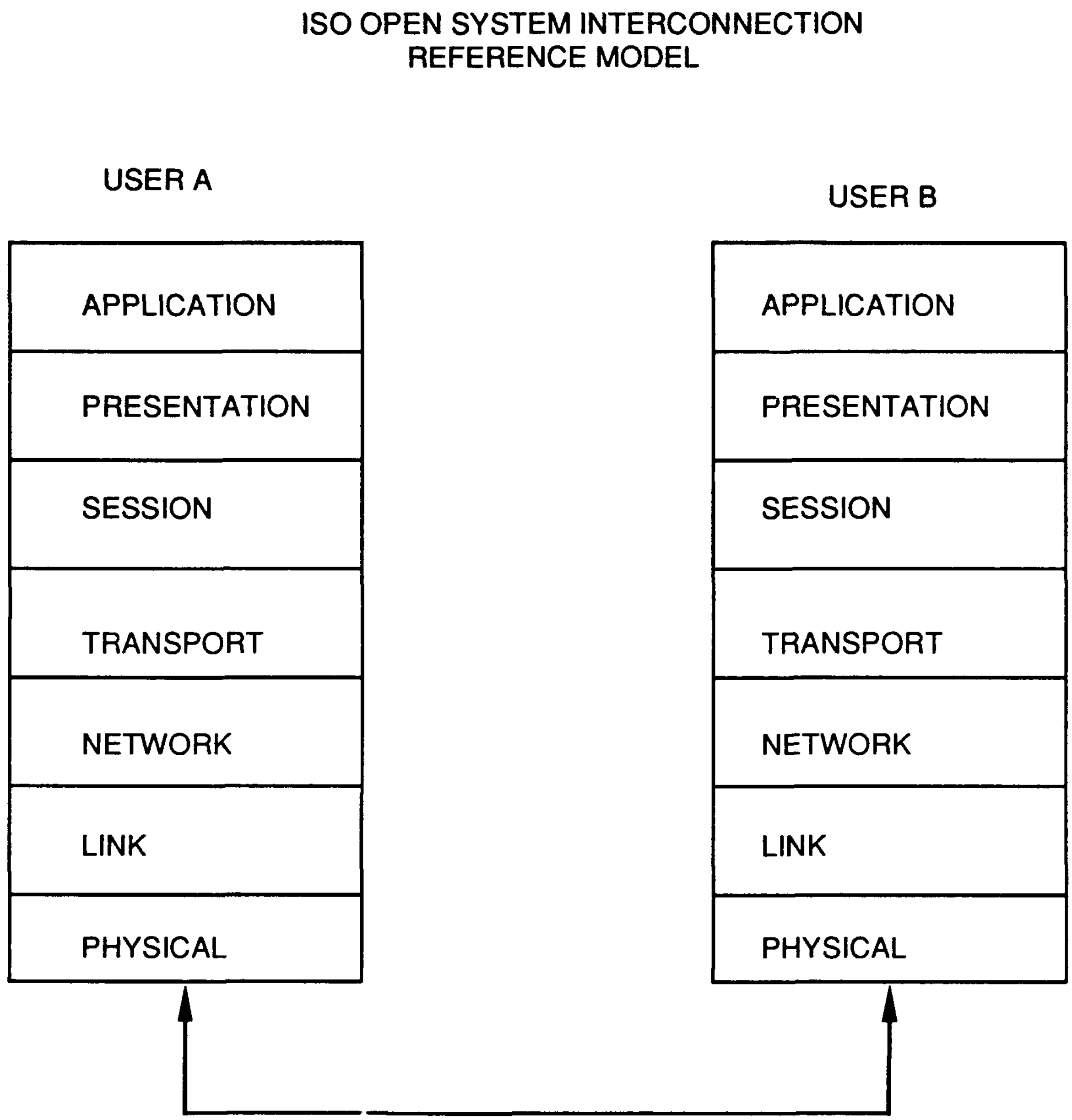
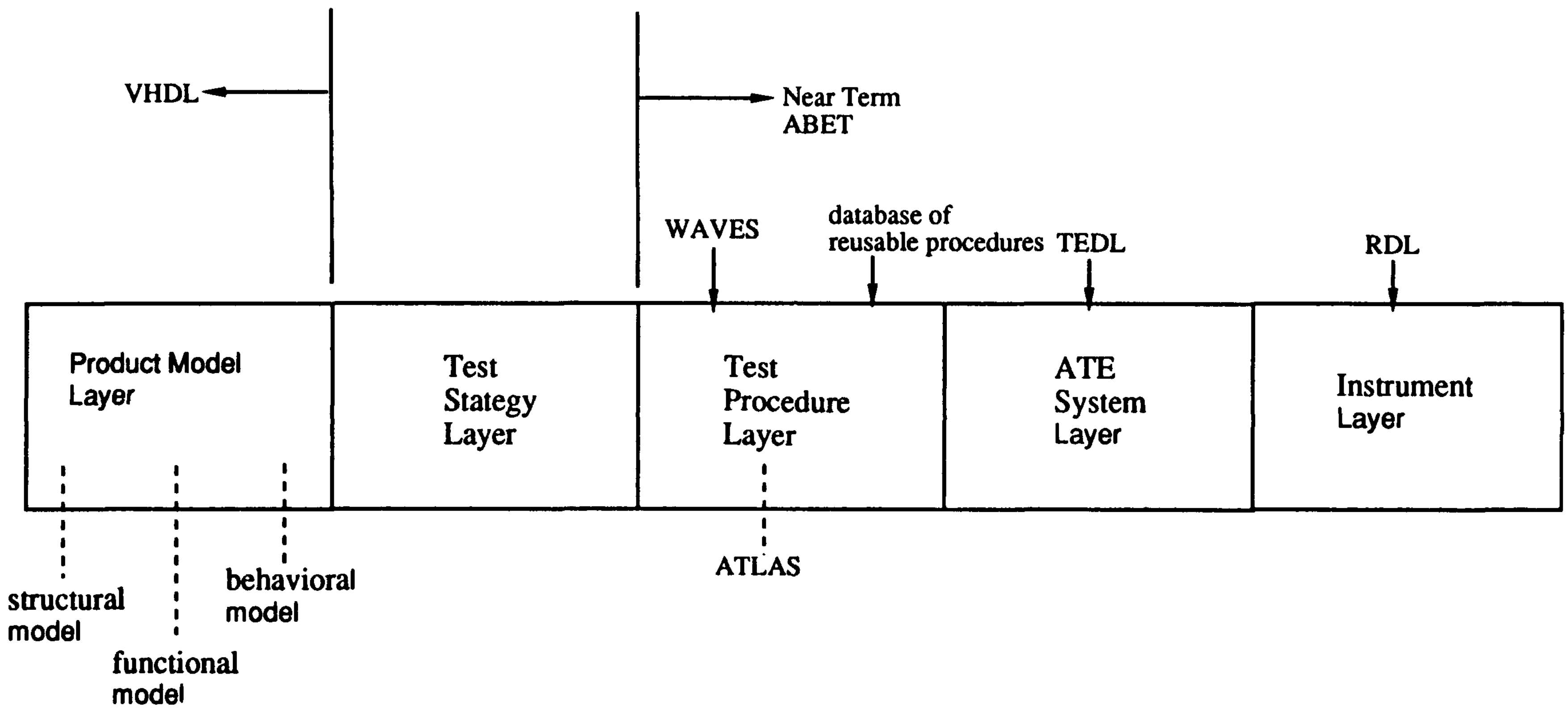


Figure 3. OSI Reference Model

Current Emphasis



from Oct 1990 working draft Volume One - ABET Architecture

"4.3 The Test Strategy Standards
Note: The standards explicitely associated with the test strategy are not implemented in the current issue of ABET."

Figure 4. Projects Within SCC20

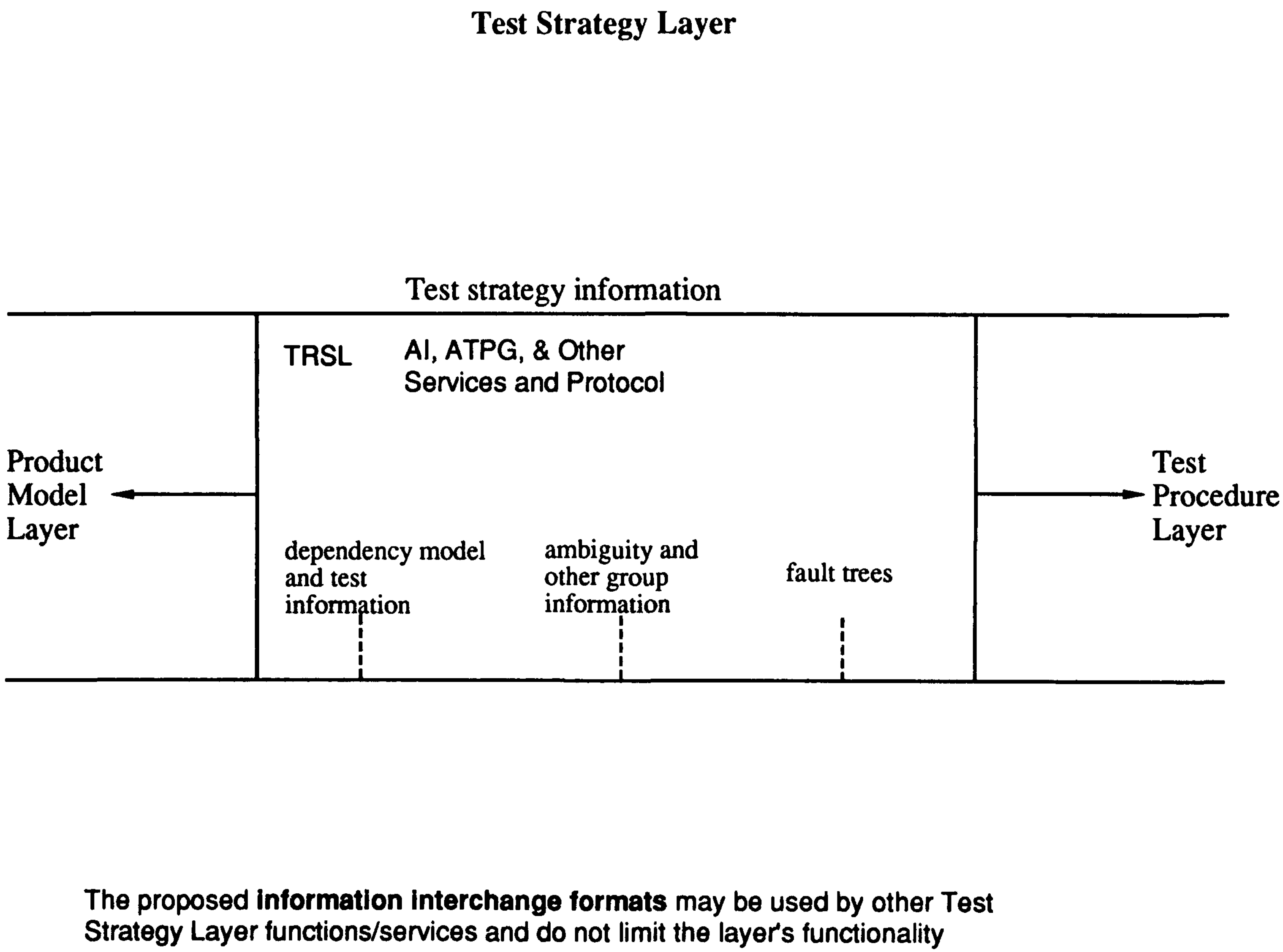


Figure 5. Expansion of the SCC20 Test Strategy Layer

Current RAM Tools

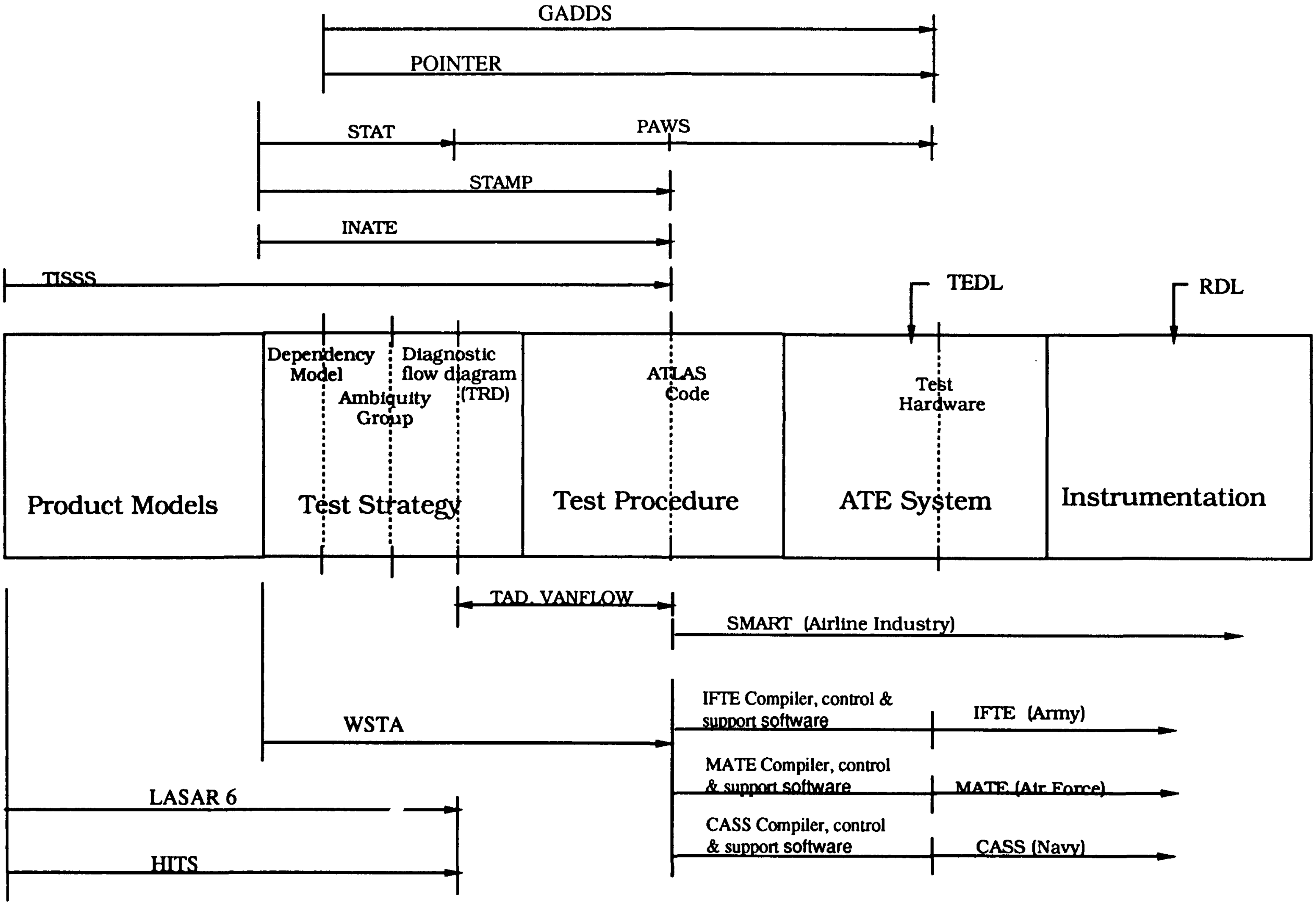
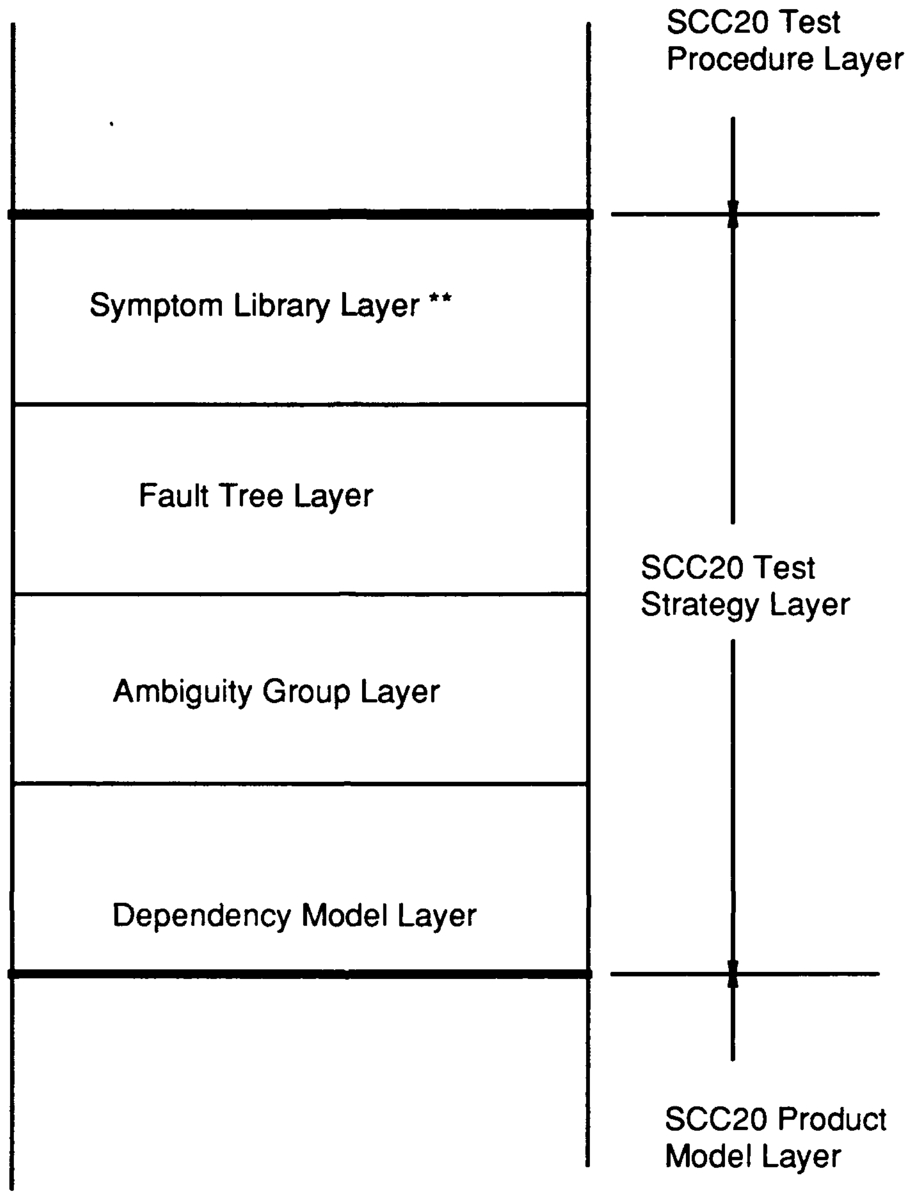


Figure 6. Concurrent Tools and Their Relationship to the SCC20 Open Architecture



** The Symptom Library Level is Under Consideration - No work has been done to define this layer within the SCC20 Open Architecture

Figure 7. Proposed Structure Within Test Strategy Layer

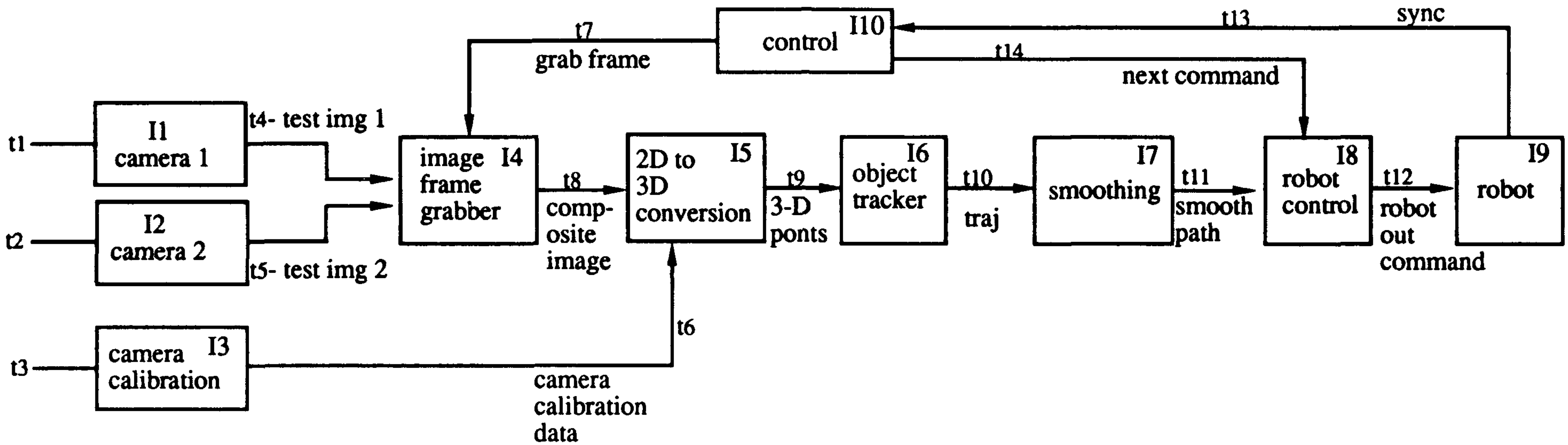


Figure 8. Robot Hand-Eye Coordination System System Level Diagram

Robotic Hand_eye Coordination System
System Level Example

t4	l1	t1		
t5	l2	t2		
t6	l5	t8		
t7	l10	t13		
t8	l4	t4	t5	t7
t9	l5	t8	t6	
t10	l6	t9		
t11	l7	t10		
t12	l8	t11	t14	
t13	l9	t12		
t14	l10	t13		

For Each Test Enter

Time to Test
Cost to Test
Test Reliability
Technicians required
Equipment Required
Test Group Data

For Each Part Enter

Time to Replace
Cost to Replace
Probability of Failure
Inventory Status

Figure 9. Dependency Model for the Robotic Hand-Eye Coordination System

STAT I Demo Version 1.6.4 S/N: STI01060400010000546
Thu Feb 07 19:13:51 1980 Page 0003
SYSTEM 8: trypipe1
MODEL 2: model2 CASE 1: 1

FEEDBACK LOOP INDICATOR REPORT

SUMMARY ANALYSIS

Total Number of Feedback Loops	=	1
Probability of Failure within a Feedback Loop	=	0.51111111
% of All Items Involved in Feedback Loop(s)	=	80.00
Feedback Loop Complexity	=	0.8000

Feedback Loop Complexity Chart

```
 1.00 |
      |
      |        FLC = 0.8000
      |
      |           XXXXXX
 0.75 |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
 0.50 |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
 0.25 |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
      |           XXXXXX
 0.00  ------------------------------
             Feedback Loop
              Complexity
```

Aggregate Item Characteristics per Feedback Loop:

Feedback Loop ID#	Number of Items	Cost to Replace	Time to Replace	Failure Probability
1	++ 8	++ 5350.00	++ 211.00	++ 0.51111111
TOTALS:	8	5350.00	211.00	
AVERAGE:	8.00	5350.00	211.00	

Figure 10. Output of STAT

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Statistics to Isolate a Primary Failure:

Number of Tests:	MINIMUM	=	3	
	MAXIMUM	=	5	
	AVERAGE	=	4.00	
Test Cost:	MINIMUM	=	5.00	
	MAXIMUM	=	9.00	
	AVERAGE	=	7.29	
Test Time:	MINIMUM	=	5.00	minutes
	MAXIMUM	=	9.00	minutes
	AVERAGE	=	7.29	minutes
Number of Enclosures:	MINIMUM	=	1	
	MAXIMUM	=	1	
	AVERAGE	=	1.00	

Dynamic Item Involvement Ratio Statistics

Without Failure Rates:		With Failure Rates:	
MINIMUM =	0.25000000	MINIMUM =	0.00555556
MAXIMUM =	0.25000000	MAXIMUM =	0.11111111

Figure 11. Output of STAT

SYSTEM 8: trypipel
MODEL 2: model2 CASE 1: 1

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Table

	Record	Cfg-Test	-Asp	Page	Previous Record	Next Diagnostic Step			(Record)
*	1.	1-T15	-1	9		GOOD: No Faults Encountered			
						BAD: Goto	1-T6	-1	(2)
	2.	1-T6	-1	9	1	GOOD: Goto	1-T5	-1	(4)
						BAD: Goto	1-T3	-1	(3)
	3.	1-T3	-1	9	2	GOOD: Replace SAG Ref # 1			
						BAD: Faulty Input			
	4.	1-T5	-1	10	2	GOOD: Goto	1-T4	-1	(6)
						BAD: Goto	1-T2	-1	(5)
	5.	1-T2	-1	10	4	GOOD: Replace SAG Ref # 2			
						BAD: Faulty Input			
	6.	1-T4	-1	11	4	GOOD: Replace SAG Ref # 4			
						BAD: Goto	1-T1	-1	(7)
	7.	1-T1	-1	11	6	GOOD: Replace SAG Ref # 3			
						BAD: Faulty Input			

Figure 12. Optimal Test Flow for Example 2.

SYSTEM 8: trypipel
MODEL 2: model2 CASE 2: case2

BREAKPOINT CANDIDATES LISTING

Feedback Loop 1 of 1

Breakpoint Candidates Test	-Asp	Description	# of AGs	AG Size Min	Max	Avg
T8	-1	composite_image	6	1	4	1.50
T9	-1	3-D point	6	1	4	1.50
T7	-1	grab_frame_signal	6	1	4	1.50
T10	-1	trajectory	6	1	4	1.50
T11	-1	smooth_path	6	1	4	1.50
T13	-1	sync_signal	8*	1	2*	1.12*
T14	-1	command_to_robot	2	2	7	4.50
T12	-1	robot_control_signs	8*	1	2*	1.12*

END OF LISTING

Figure 13. Breakpoint Candidates for Example 2.

STAT I Demo Version 1.6.4 S/N: STI01060400010000546

Thu Feb 07 19:47:16 1980 Page 0003
SYSTEM 8: trypipe1
MODEL 2: model2

FEEDBACK LOOP INDICATOR REPORT

SUMMARY ANALYSIS

Total Number of Feedback Loops	=	1
Probability of Failure within a Feedback Loop	=	0.33333333
% of All Items Involved in Feedback Loop(s)	=	40.00
Feedback Loop Complexity	=	0.4000

Feedback Loop Complexity Chart

```
 1.00 |
      |
      |
      |
 0.75 |
      |
      |
      |
 0.50 |          FLC = 0.4000
      |             XXXXXX
      |             XXXXXX
      |             XXXXXX
 0.25 |             XXXXXX
      |             XXXXXX
      |             XXXXXX
      |             XXXXXX
      |             XXXXXX
 0.00  --------------------------------
               Feedback Loop
                Complexity
```

Aggregate Item Characteristics per Feedback Loop:

Feedback Loop ID#	Number of Items	Cost to Replace	Time to Replace	Failure Probability
1	++ 4	++ 2450.00	++ 101.00	++ 0.33333333
TOTALS:	4	2450.00	101.00	
AVERAGE:	4.00	2450.00	101.00	

END OF REPORT

Figure 14.
RESULTS FROM BREAKING FEEDBACK LOOP AT T7

SYSTEM 8: trypipe1
MODEL 2: model2 CASE 1: 1

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Dynamic Ambiguity Group Statistics:

Total Unique Ambiguity Group Size(s): 2

Total Unique Ambiguity Group(s): 4

Total Ambiguity Group(s): 4

Size	Ambiguity Group Unique Qty	Ambiguity Group Total Qty	Relative Isolation Levels size %	Relative Isolation Levels cum %	Relative Failure Probability size %	Relative Failure Probability cum %
1	3	3	75.00	75.00	53.33	53.33
7	1	1	25.00	100.00	46.67	100.00

Figure 15. Results from Breaking Loop at T7

SYSTEM 8: trypipel
MODEL 2: model2

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Dynamic Ambiguity Group Statistics:

Total Unique Ambiguity Group Size(s): 1

Total Unique Ambiguity Group(s): 10

Total Ambiguity Group(s): 10

Size	Ambiguity Group Unique Qty	Ambiguity Group Total Qty	Relative Isolation Levels size %	Relative Isolation Levels cum %	Relative Failure Probability size %	Relative Failure Probability cum %
1	10	10	100.00	100.00	100.00	100.00

Figure 16.
RESULTS FROM BREAKING FEEDBACK LOOP AT T13

STAT I Demo Version 1.6.4 S/N: STI01060400010000546
Thu Feb 07 19:56:33 1980 Page 0003
SYSTEM 8: trypipe1
MODEL 2: model2

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Statistics to Isolate a Primary Failure:

Number of Tests:	MINIMUM	=	4	
	MAXIMUM	=	6	
	AVERAGE	=	4.92	
Test Cost:	MINIMUM	=	5.00	
	MAXIMUM	=	11.00	
	AVERAGE	=	8.62	
Test Time:	MINIMUM	=	5.00	minutes
	MAXIMUM	=	11.00	minutes
	AVERAGE	=	8.62	minutes
Number of Enclosures:	MINIMUM	=	1	
	MAXIMUM	=	1	
	AVERAGE	=	1.00	

Dynamic Item Involvement Ratio Statistics

Without Failure Rates:		With Failure Rates:	
MINIMUM =	0.10000000	MINIMUM =	0.00222222
MAXIMUM =	0.10000000	MAXIMUM =	0.04444444

Figure 17. STAT Outputs for Example 2 with Loop Broken at T13

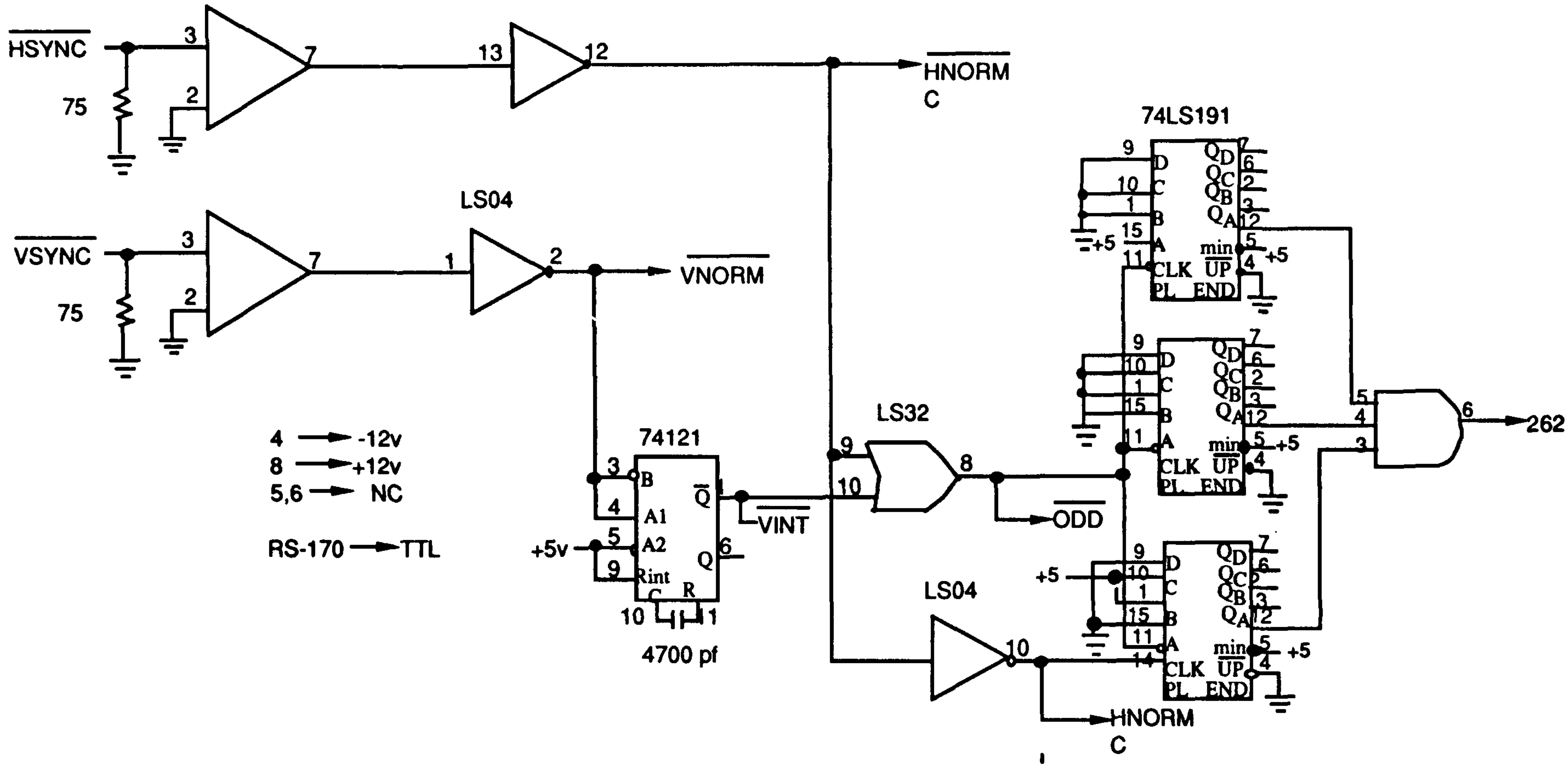
FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Table

	Record	Cfg-Test	-Asp	Page	Previous Record	Next Diagnostic Step				(Record)
*	1.	1-T15	-1	9		GOOD: No Faults Encountered				
						BAD: Goto	1-T8	-1	(	2)
	2.	1-T8	-1	9	1	GOOD: Goto	1-T10	-1	(	9)
						BAD: Goto	1-T7	-1	(	3)
	3.	1-T7	-1	9	2	GOOD: Goto	1-T5	-1	(	5)
						BAD: Goto	1-T13	-1	(	4)
	4.	1-T13	-1	9	3	GOOD: Replace SAG Ref # 2				
						BAD: Replace SAG Ref # 1				
	5.	1-T5	-1	10	3	GOOD: Goto	1-T4	-1	(	7)
						BAD: Goto	1-T2	-1	(	6)
	6.	1-T2	-1	10	5	GOOD: Replace SAG Ref # 3				
						BAD: Faulty Input				
	7.	1-T4	-1	11	5	GOOD: Replace SAG Ref # 5				
						BAD: Goto	1-T1	-1	(	8)
	8.	1-T1	-1	11	7	GOOD: Replace SAG Ref # 4				
						BAD: Faulty Input				
	9.	1-T10	-1	12	2	GOOD: Goto	1-T11	-1	(	13)
						BAD: Goto	1-T9	-1	(	10)
	10.	1-T9	-1	12	9	GOOD: Replace SAG Ref # 8				
						BAD: Goto	1-T6	-1	(	11)
	11.	1-T6	-1	12	10	GOOD: Replace SAG Ref # 7				
						BAD: Goto	1-T3	-1	(	12)
	12.	1-T3	-1	12	11	GOOD: Replace SAG Ref # 6				
						BAD: Faulty Input				
	13.	1-T11	-1	14	9	GOOD: Replace SAG Ref # 10				
						BAD: Replace SAG Ref # 9				

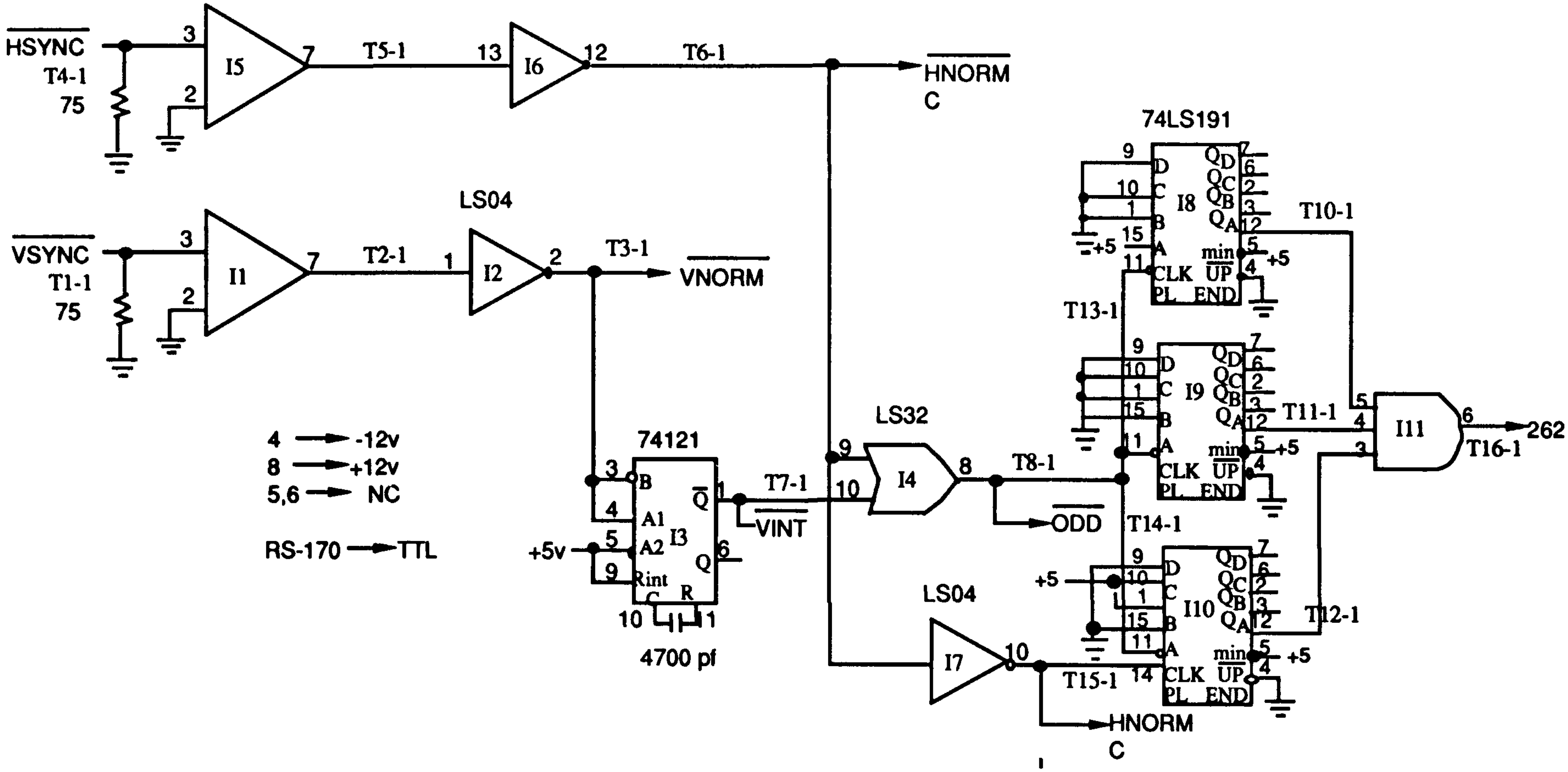
Figure 18. Optimal Fault Tree for Example 2.



This portion of the circuit converts the RS-170 signals into TTL levels, and generates a short pulse (4 sec) whenever the falling edges of HSYNC and VSYNC align, in other words, the start of the odd field. (VINT is used in the interrupt circuit)

This portion loads a down counter with 262, counts down 262 HSYNC periods and generates a signal to enable the creation of the fake VSYNC. This VFAKE signal will then precede the normal even field VSYNC by 1/2 HSYNC.

Figure 19. Interlaced/Non-Interlaced Sync Signal Generation Circuit



This portion of the circuit converts the RS-170 signals into TTL levels, and generates a short pulse (4 sec) whenever the falling edges of HSYNC and VSYNC align, in other words, the start of the odd field. (VINT is used in the interrupt circuit)

This portion loads a down counter with 262, counts down 262 HSYNC periods and generates a signal to enable the creation of the fake VSYNC. This VFAKE signal will then precede the normal even field VSYNC by 1/2 HSYNC.

Figure 19. Continued

SYSTEM 1: test_system
MODEL 2: non-interlaced_sync_box CASE 10: base case

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Statistics to Isolate a Primary Failure:

Number of Tests:	MINIMUM	=	2	
	MAXIMUM	=	7	
	AVERAGE	=	5.45	
Test Cost:	MINIMUM	=	2.00	
	MAXIMUM	=	13.00	
	AVERAGE	=	9.82	
Test Time:	MINIMUM	=	2.00	minutes
	MAXIMUM	=	13.00	minutes
	AVERAGE	=	9.82	minutes
Number of Enclosures:	MINIMUM	=	1	
	MAXIMUM	=	1	
	AVERAGE	=	1.00	

Dynamic Item Involvement Ratio Statistics

Without Failure Rates:		With Failure Rates:	
MINIMUM =	0.05263158	MINIMUM =	0.00021265
MAXIMUM =	0.05263158	MAXIMUM =	0.01063264

Figure 20. STAT Output for Example 3.

SYSTEM 1: test_system
MODEL 2: non-interlaced_sync_box CASE 10: base case

FAULT ISOLATION INDICATOR REPORT

SUMMARY ANALYSIS

Dynamic Ambiguity Group Statistics:

Total Unique Ambiguity Group Size(s): 2

Total Unique Ambiguity Group(s): 19

Total Ambiguity Group(s): 19

Size	Ambiguity Group Unique Qty	Ambiguity Group Total Qty	Relative Isolation Levels size %	Relative Isolation Levels cum %	Relative Failure Probability size %	Relative Failure Probability cum %
1	18	18	94.74	94.74	99.19	99.19
2	1	1	5.26	100.00	0.81	100.00

Figure 21. STAT Output for Example 3.

Wed Feb 06 20:10:28 1980
SYSTEM 1: test_system
MODEL 2: non-interlaced_sync_box CASE 10: base case

FEEDBACK LOOP INDICATOR REPORT

SUMMARY ANALYSIS

Total Number of Feedback Loops	=	1
Probability of Failure within a Feedback Loop	=	0.00808081
% of All Items Involved in Feedback Loop(s)	=	10.00
Feedback Loop Complexity	=	0.1000

Feedback Loop Complexity Chart

```
1.00  |
      |
      |
      |
0.75  |
      |
      |
      |
0.50  |
      |
      |
      |
0.25  |
            FLC = 0.1000
      |
               XXXXXX
      |        XXXXXX
0.00   ------------------------------
            Feedback Loop
             Complexity
```

Aggregate Item Characteristics per Feedback Loop:

Feedback Loop ID#	Number of Items	Cost to Replace	Time to Replace	Failure Probability
1	++ 2	++ 2.00	++ 4.00	++ 0.00808081
TOTALS:	2	2.00	4.00	
AVERAGE:	2.00	2.00	4.00	

END OF REPORT

Figure 22. STAT Output for Example 3.

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Table

	Record	Cfg-Test	-Asp	Page	Previous Record	Next Diagnostic Step	(Record)
*	1.	1-T26	-1	9		GOOD: Goto 1-T27 -1	(22)
						BAD: Goto 1-T25 -1	(2)
	2.	1-T25	-1	9	1	GOOD: Goto 1-T16 -1	(13)
						BAD: Goto 1-T8 -1	(3)
	3.	1-T8	-1	9	2	GOOD: Goto 1-T23 -1	(11)
						BAD: Goto 1-T7 -1	(4)
	4.	1-T7	-1	9	3	GOOD: Goto 1-T6 -1	(8)
						BAD: Goto 1-T3 -1	(5)
	5.	1-T3	-1	9	4	GOOD: Replace SAG Ref # 3	
						BAD: Goto 1-T2 -1	(6)
	6.	1-T2	-1	10	5	GOOD: Replace SAG Ref # 2	
						BAD: Goto 1-T1 -1	(7)
	7.	1-T1	-1	10	6	GOOD: Replace SAG Ref # 1	
						BAD: Faulty Input	
	8.	1-T6	-1	11	4	GOOD: Replace SAG Ref # 6	
						BAD: Goto 1-T5 -1	(9)
	9.	1-T5	-1	11	8	GOOD: Replace SAG Ref # 5	
						BAD: Goto 1-T4 -1	(10)
	10.	1-T4	-1	12	9	GOOD: Replace SAG Ref # 4	
						BAD: Faulty Input	
	11.	1-T23	-1	13	3	GOOD: Replace SAG Ref # 8	
						BAD: Goto 1-T22 -1	(12)
	12.	1-T22	-1	13	11	GOOD: Replace SAG Ref # 7	
						BAD: Faulty Input	
	13.	1-T16	-1	14	2	GOOD: Goto 1-T19 -1	(18)
						BAD: Goto 1-T13 -1	(14)
	14.	1-T13	-1	14	13	GOOD: Goto 1-T10 -1	(17)
						BAD: Goto 1-T14 -1	(15)
	15.	1-T14	-1	14	14	GOOD: Replace SAG Ref # 11	
						BAD: Goto 1-T15 -1	(16)
	16.	1-T15	-1	14	15	GOOD: Replace SAG Ref # 10	
						BAD: Replace SAG Ref # 9	
	17.	1-T10	-1	16	14	GOOD: Replace SAG Ref # 13	
						BAD: Replace SAG Ref # 12	

Figure 23. Fault Tree for Example 3.

	18.	1-T19	-1	17	13	GOOD: Goto	1-T20	-1	(	21)
						BAD: Goto	1-T18	-1	(	19)
	19.	1-T18	-1	17	18	GOOD: Replace SAG Ref # 16				
						BAD: Goto	1-T17	-1	(	20)
	20.	1-T17	-1	17	19	GOOD: Replace SAG Ref # 15				
						BAD: Replace SAG Ref # 14				
	21.	1-T20	-1	18	18	GOOD: Replace SAG Ref # 18				
						BAD: Replace SAG Ref # 17				
*	22.	1-T27	-1	19	1	GOOD: No Faults Encountered				
						BAD: Replace SAG Ref # 19				

Figure 23. Continued

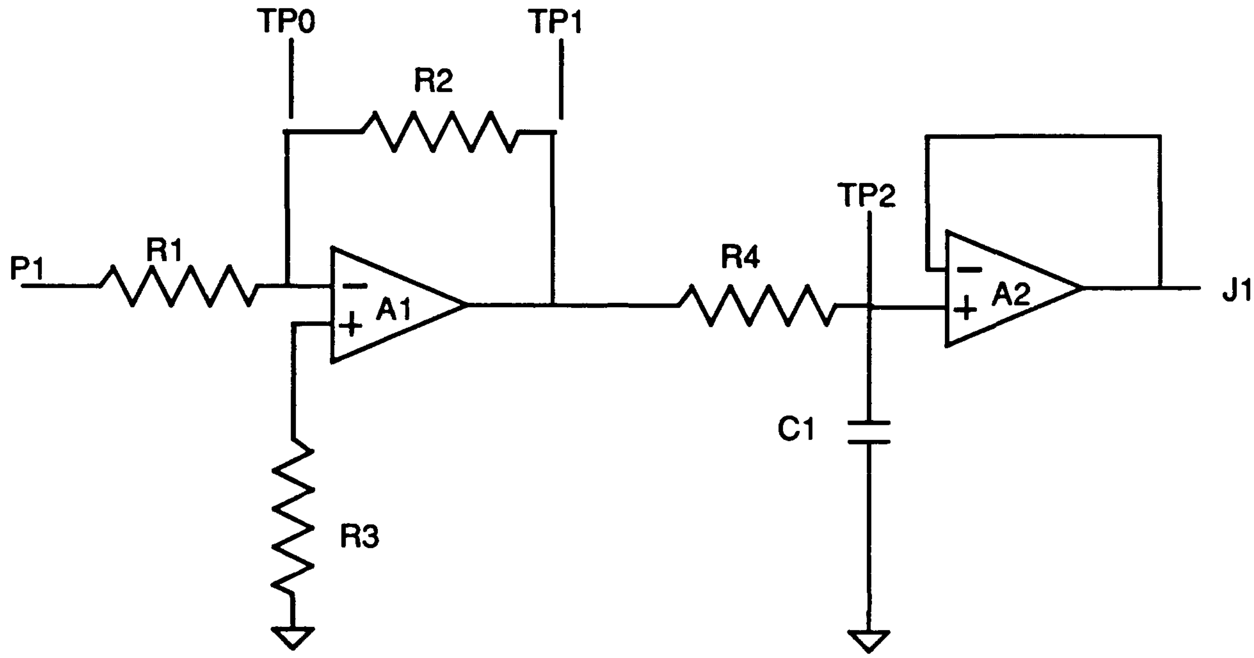


Figure 24. Circuit Diagram for Example 4.

Tools or ABET Services Facilitated by Information Exchange Standards

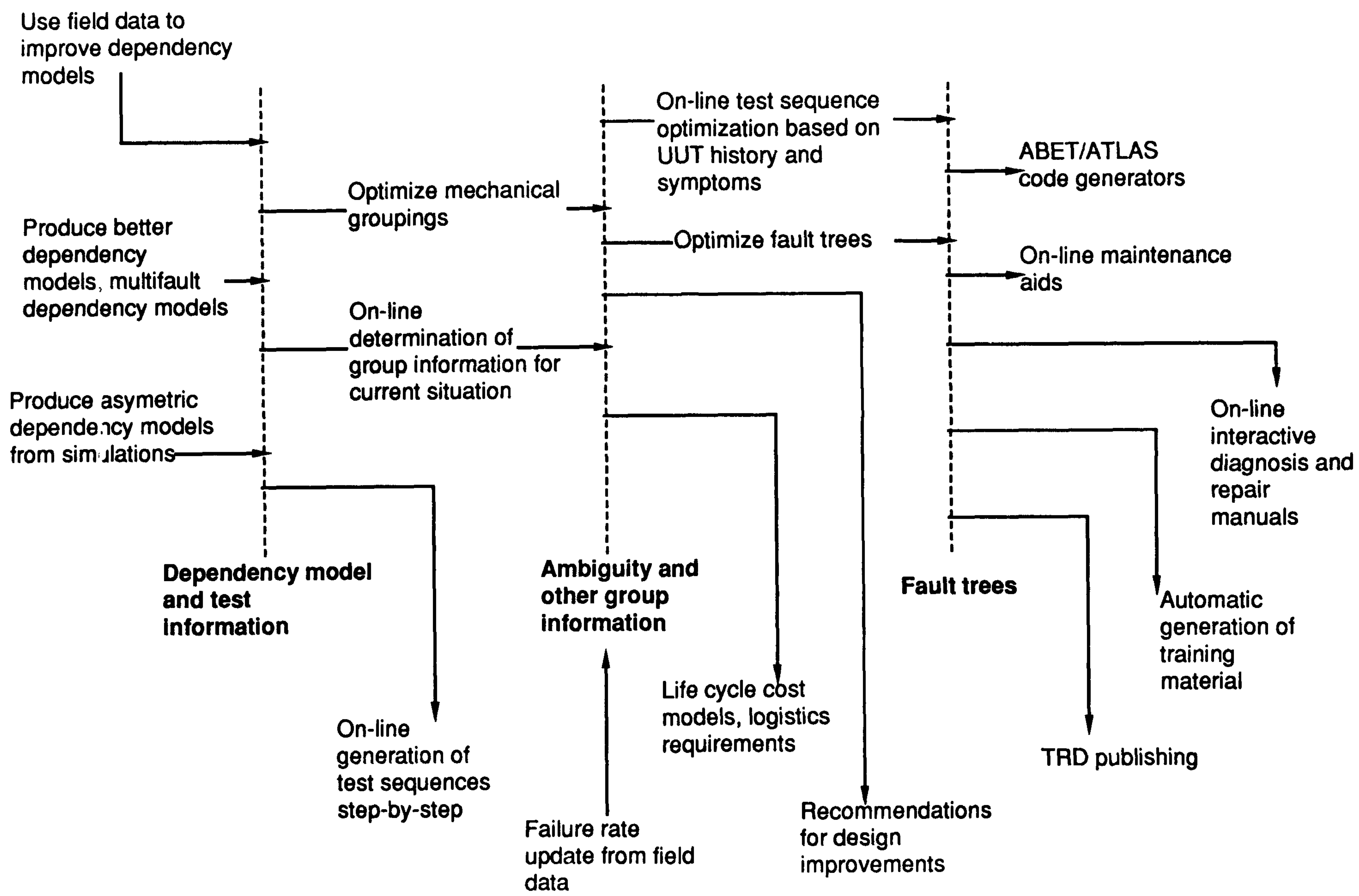


Figure 26. Tools Which Would Benefit From Open Architectu

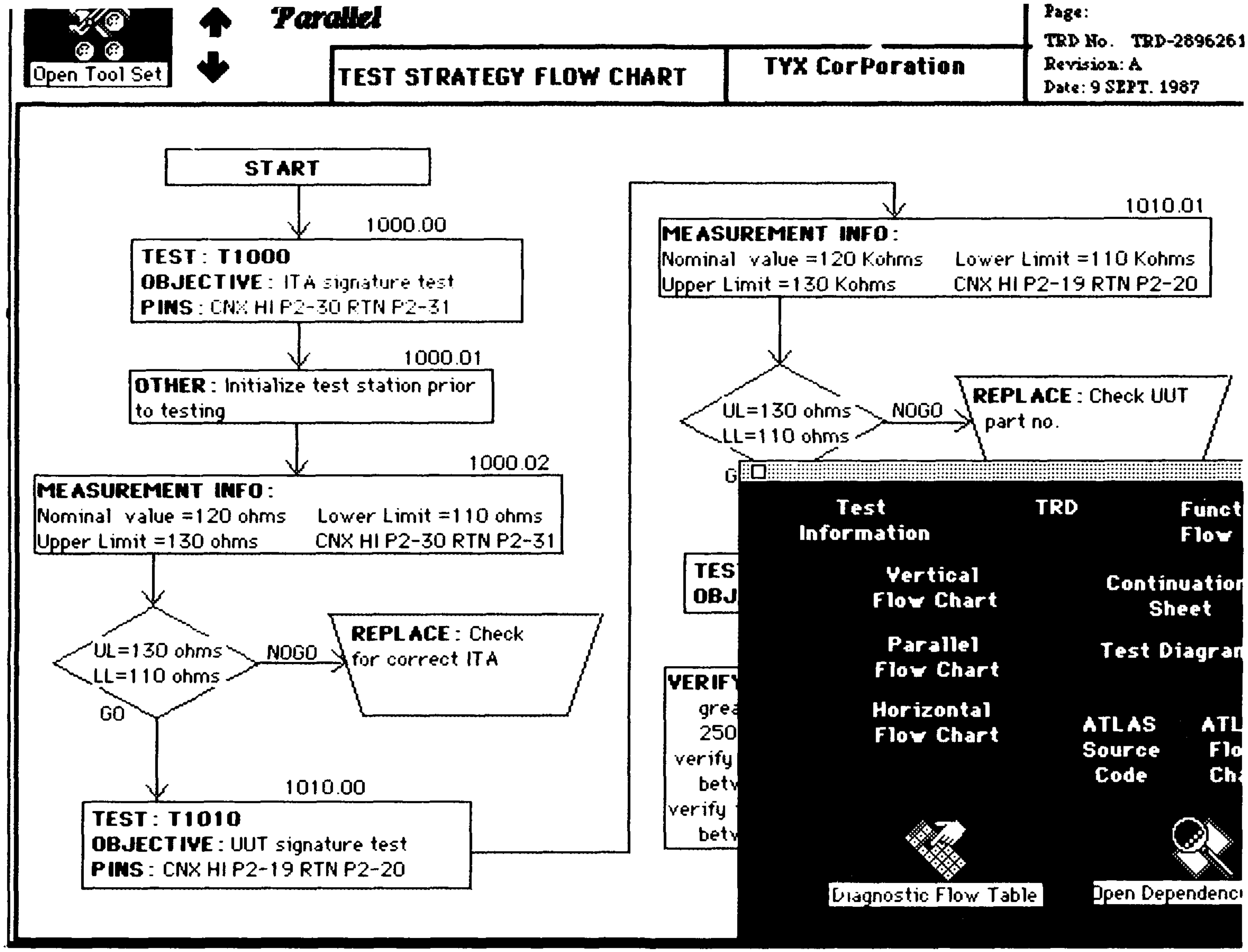

Open Tool Set
Parallel
TEST STRATEGY FLOW CHART
TYX CorPoration
Page:
TRD No. TRD-2896261
Revision: A
Date: 9 SEPT. 1987
START
1000.00
TEST : T1000
OBJECTIVE : ITA signature test
PINS : CNX HI P2-30 RTN P2-31
1000.01
OTHER : Initialize test station prior to testing
1000.02
MEASUREMENT INFO :
Nominal value =120 ohms Lower Limit =110 ohms
Upper Limit =130 ohms CNX HI P2-30 RTN P2-31
UL=130 ohms
LL=110 ohms
NOGO
GO
REPLACE : Check for correct ITA
1010.00
TEST : T1010
OBJECTIVE : UUT signature test
PINS : CNX HI P2-19 RTN P2-20
1010.01
MEASUREMENT INFO :
Nominal value =120 Kohms Lower Limit =110 Kohms
Upper Limit =130 Kohms CNX HI P2-19 RTN P2-20
UL=130 ohms
LL=110 ohms
NOGO
REPLACE : Check UUT part no.
Test Information
TRD
Vertical Flow Chart
Parallel Flow Chart
Horizontal Flow Chart
Continuation Sheet
Test Diagram
ATLAS Source Code
Diagnostic Flow Table

Figure 27.

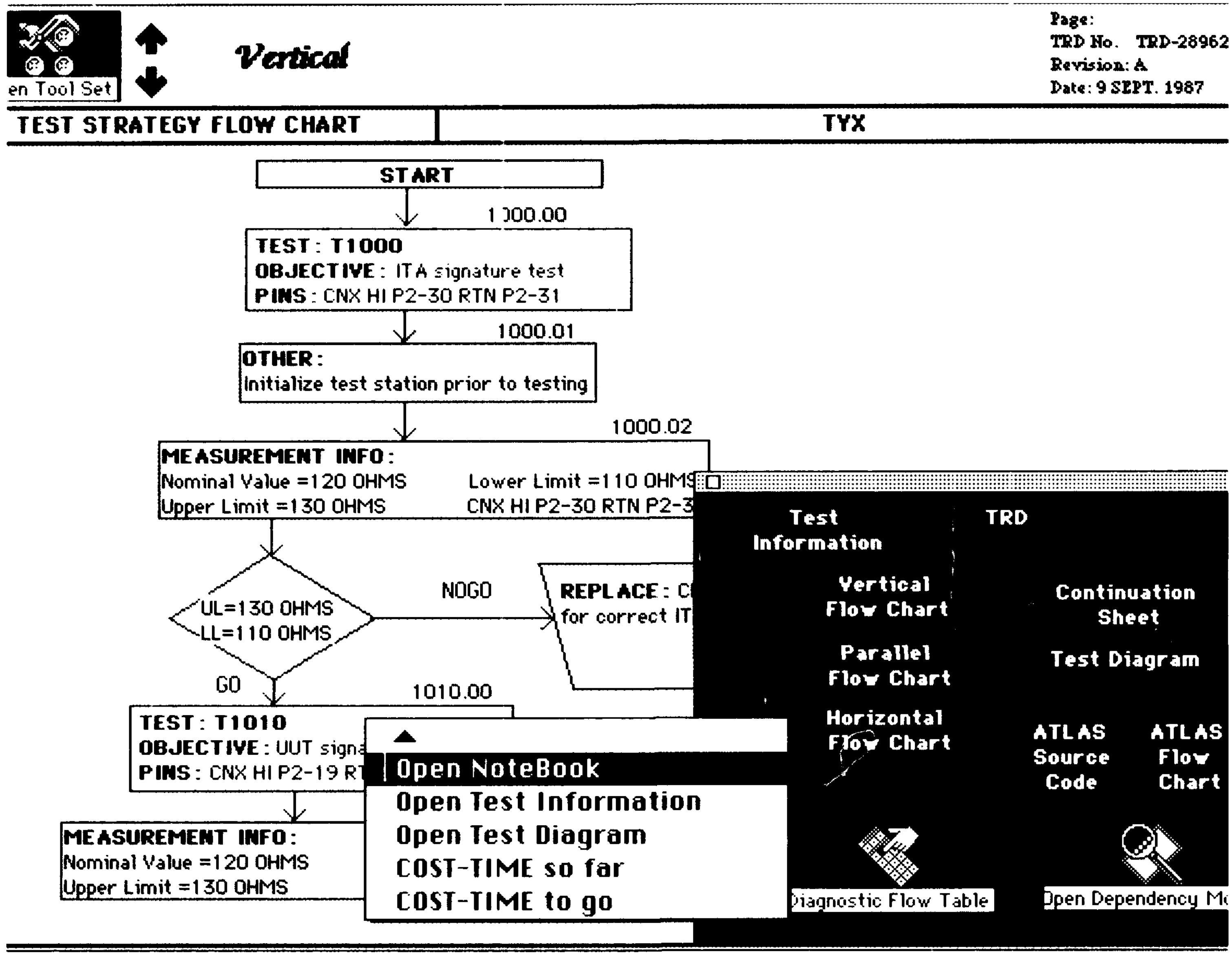

en Tool Set
Vertical
Page:
TRD No. TRD-28962
Revision: A
Date: 9 SEPT. 1987
TEST STRATEGY FLOW CHART
TYX
START
1000.00
TEST : T1000
OBJECTIVE : ITA signature test
PINS : CNX HI P2-30 RTN P2-31
1000.01
OTHER :
Initialize test station prior to testing
1000.02
MEASUREMENT INFO :
Nominal Value =120 OHMS
Upper Limit =130 OHMS
Lower Limit =110 OHMS
UL=130 OHMS
LL=110 OHMS
NOGO
REPLACE :
for correct IT
GO
1010.00
TEST : T1010
OBJECTIVE : UUT signa
MEASUREMENT INFO :
Nominal Value =120 OHMS
Upper Limit =130 OHMS
Open NoteBook
Open Test Information
Open Test Diagram
COST-TIME so far
COST-TIME to go
Test Information
TRD
Vertical Flow Chart
Continuation Sheet
Parallel Flow Chart
Test Diagram
Horizontal Flow Chart
ATLAS Source Code
ATLAS Flow Chart
Diagnostic Flow Table

Figure 28.

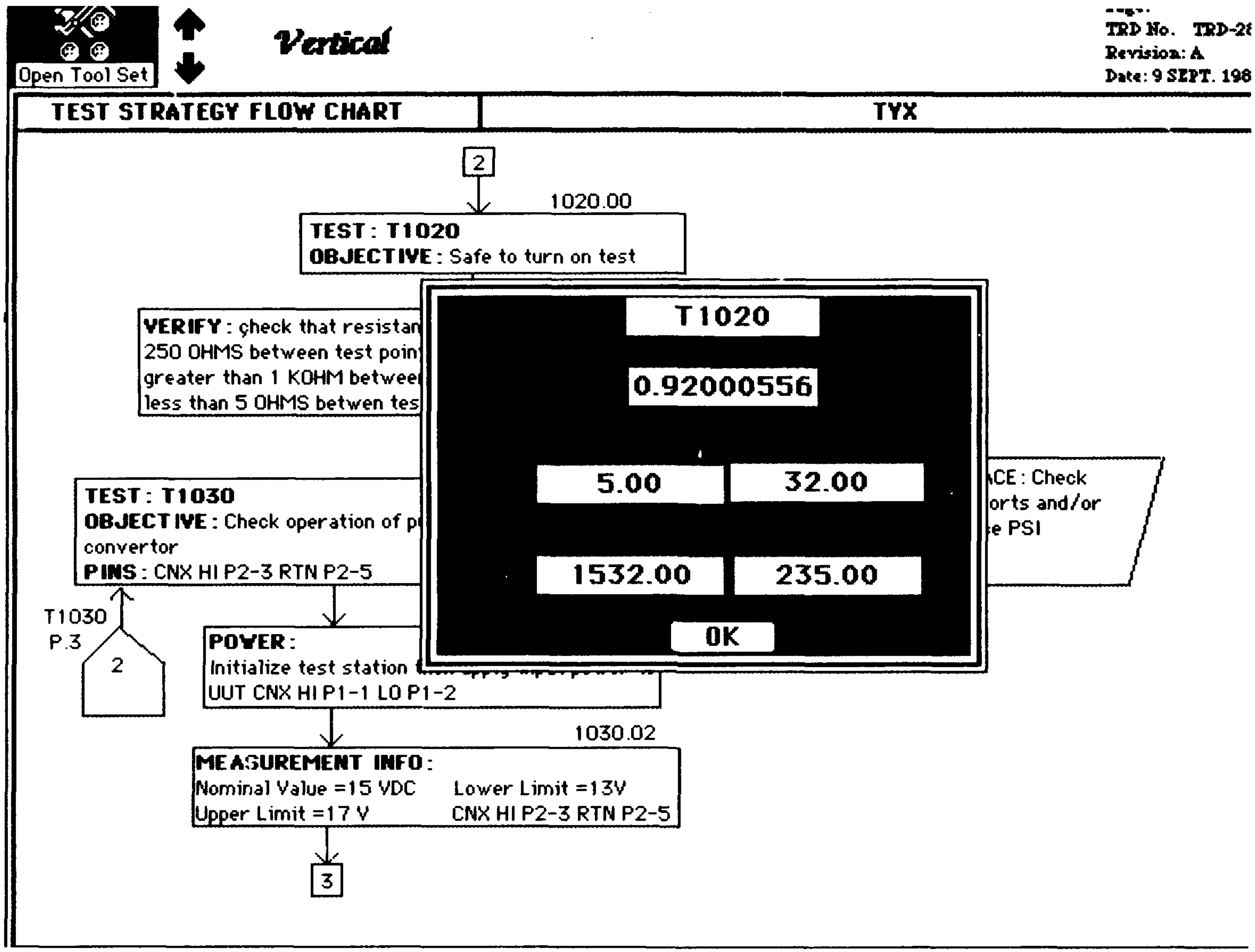

Open Tool Set
Vertical
TRD No. TRD-2
Revision: A
Date: 9 SEPT. 198
TEST STRATEGY FLOW CHART
TYX
2
1020.00
TEST : T1020
OBJECTIVE : Safe to turn on test
VERIFY : check that resistan
250 OHMS between test poin
greater than 1 KOHM betwee
less than 5 OHMS betwen tes
TEST : T1030
OBJECTIVE : Check operation of p
convertor
PINS : CNX HI P2-3 RTN P2-5
T1030
P.3
2
POWER :
Initialize test station
UUT CNX HI P1-1 LO P1-2
1030.02
MEASUREMENT INFO :
Nominal Value =15 VDC
Lower Limit =13V
Upper Limit =17 V
CNX HI P2-3 RTN P2-5
3
CE : Check
orts and/or
e PSI
T1020
0.92000556
5.00
32.00
1532.00
235.00
OK

Figure 29.

Open Tool Set

Continuation Sheet

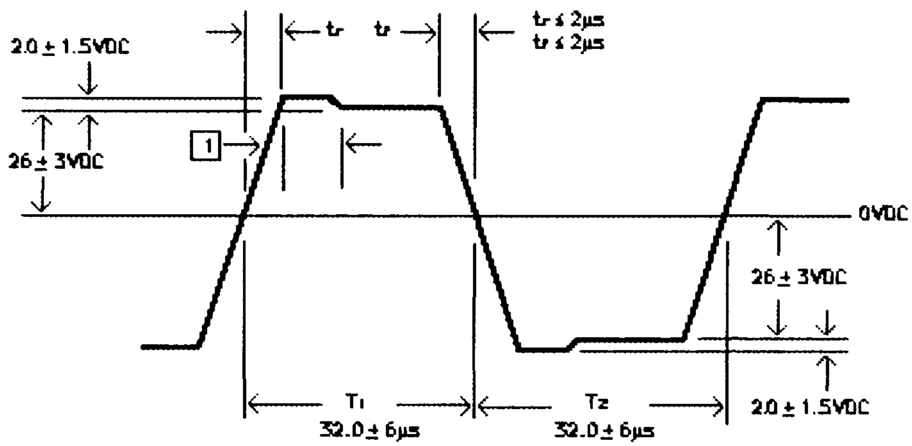
Page:
TRD No. TRD-289(
Revision: A
Date: 9 SEPT. 1987

DETAILED TEST INFORMATION
CONTINUATION SHEET

TEST NUMBER T1030

UUT **TYX DEMONSTRATION UUT**

1) The following waveform should be displayed on the test station waveform analyzer upon applicatin of input power :



2) The vertical deflection scale of the waveform analyzer should be set at 5V per devision and the horizontal set at 10USECS per division.

3) If the waveform does not conform to the above characteristics, a problem exists with the station master clock. Perform any troubleshooting and repair activities in accordance with the station amintenance and repair manual.

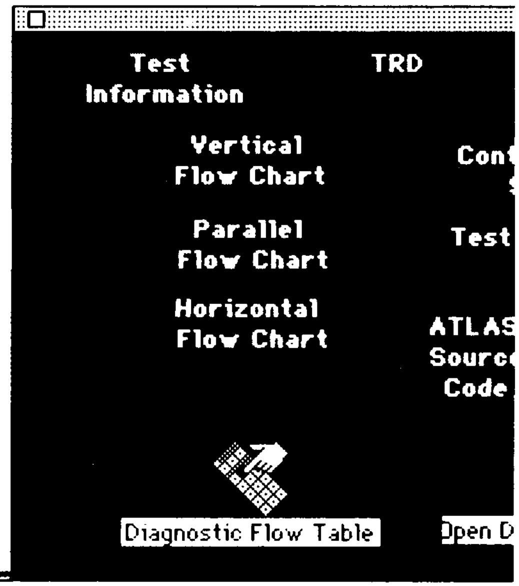


Figure 30.

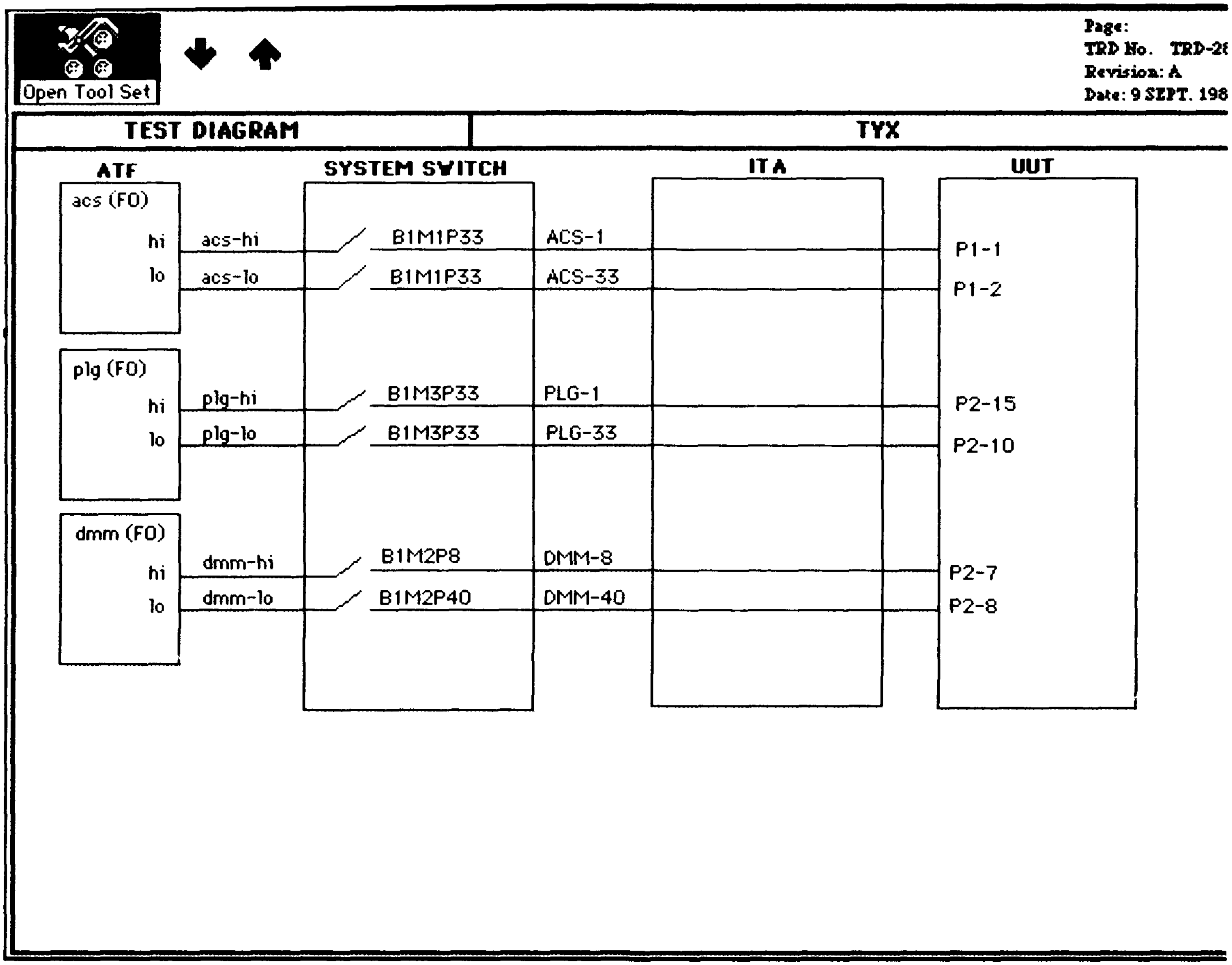

Open Tool Set
Page:
TRD No. TRD-2
Revision: A
Date: 9 SEPT. 198
TEST DIAGRAM
TYX
ATF
SYSTEM SWITCH
ITA
UUT
acs (FO)
hi
lo
acs-hi
acs-lo
B1M1P33
B1M1P33
ACS-1
ACS-33
P1-1
P1-2
plg (FO)
hi
lo
plg-hi
plg-lo
B1M3P33
B1M3P33
PLG-1
PLG-33
P2-15
P2-10
dmm (FO)
hi
lo
dmm-hi
dmm-lo
B1M2P8
B1M2P40
DMM-8
DMM-40
P2-7
P2-8

Figure 31.

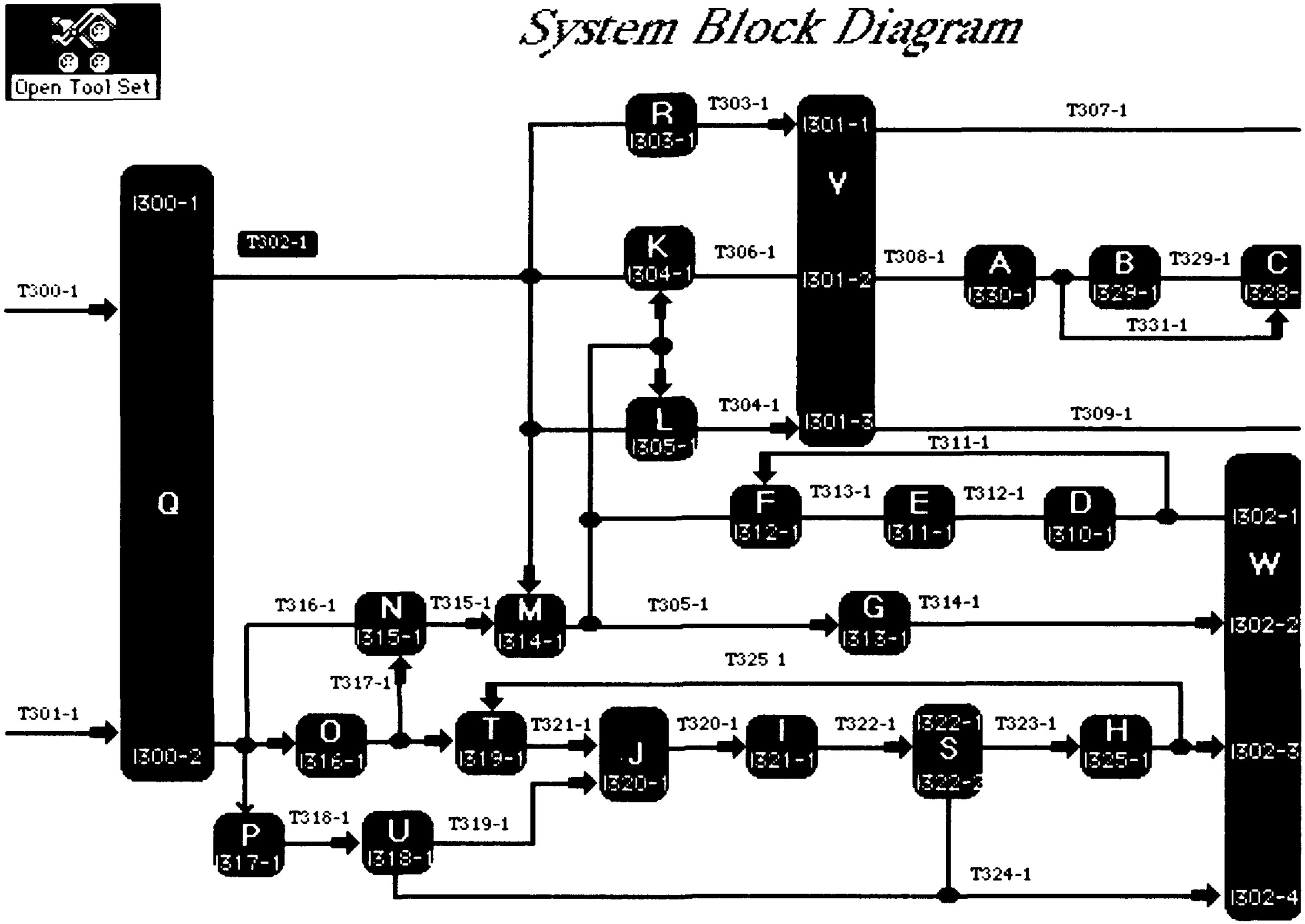
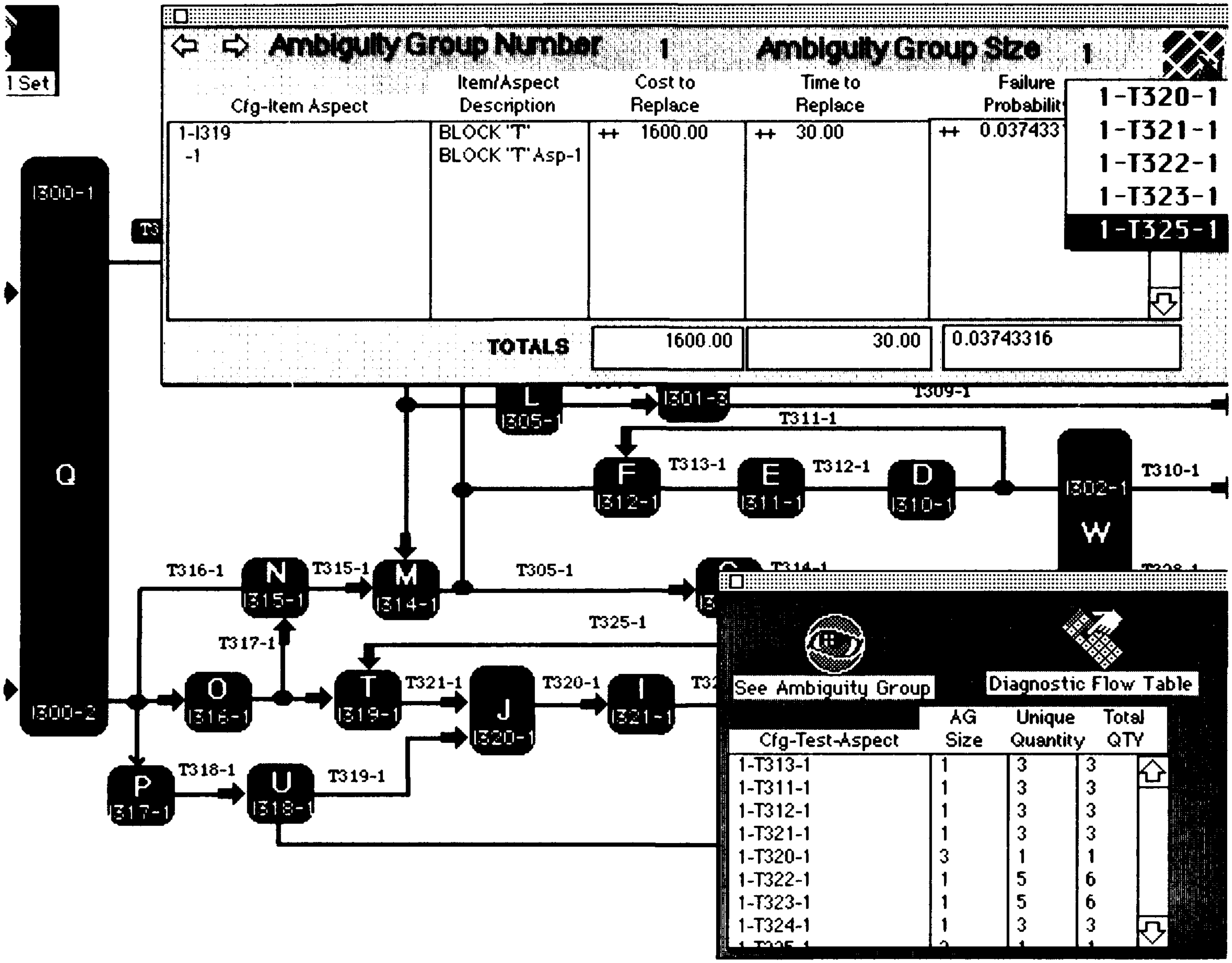
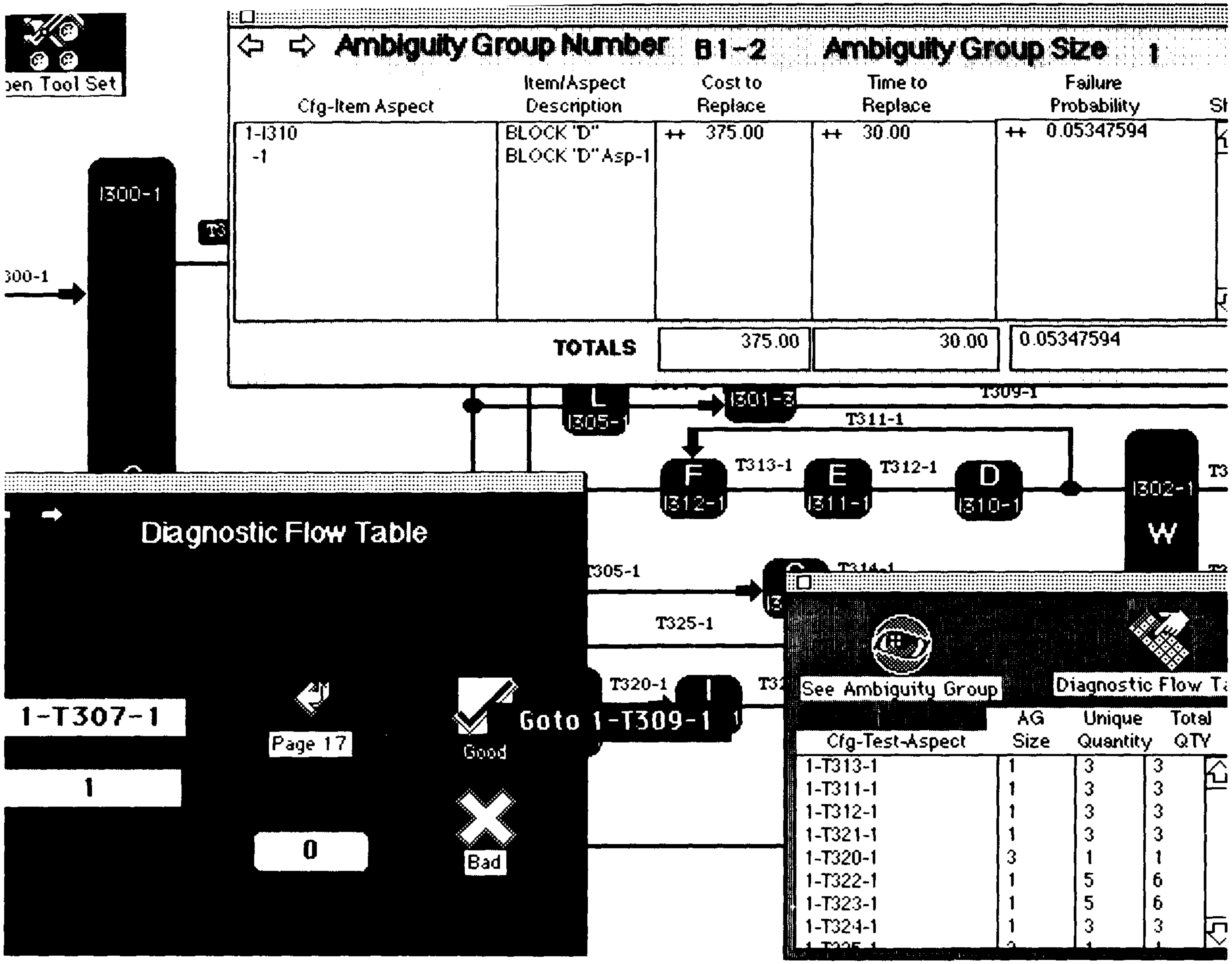

System Block Diagram
Open Tool Set
Q
I300-1
I300-2
T300-1
T301-1
T302-1
R
I303-1
T303-1
K
I304-1
T306-1
L
I305-1
T304-1
V
I301-1
I301-2
I301-3
T307-1
T308-1
T309-1
A
I330-1
B
I329-1
T329-1
C
I328-
T331-1
T311-1
F
I312-1
T313-1
E
I311-1
T312-1
D
I310-1
W
I302-1
I302-2
I302-3
I302-4
T316-1
N
I315-1
T315-1
M
I314-1
T305-1
G
I313-1
T314-1
T325 1
T317-1
O
I316-1
T
I319-1
T321-1
J
I320-1
T320-1
I
I321-1
T322-1
S
I322-1
I322-2
T323-1
H
I325-1
P
I317-1
T318-1
U
I318-1
T319-1
T324-1

Figure 32.



Ambiguity Group Number 1
Ambiguity Group Size 1
Cfg-Item Aspect
Item/Aspect Description
Cost to Replace
Time to Replace
Failure Probabilit
1-I319 -1
BLOCK 'T'
BLOCK 'T' Asp-1
1600.00
30.00
0.037433
TOTALS
1600.00
30.00
0.03743316
1-T320-1
1-T321-1
1-T322-1
1-T323-1
1-T325-1
1 Set
Q
I300-1
I300-2
L
I305-1
I301-3
T309-1
T311-1
F
I312-1
T313-1
E
I311-1
T312-1
D
I310-1
W
I302-1
T310-1
N
I315-1
M
I314-1
T316-1
T315-1
T305-1
T317-1
T325-1
O
I316-1
T
I319-1
T321-1
J
I320-1
T320-1
I
I321-1
P
I317-1
T318-1
U
I318-1
T319-1
See Ambiguity Group
Diagnostic Flow Table
Cfg-Test-Aspect
AG Size
Unique Quantity
Total QTY
1-T313-1 1 3 3
1-T311-1 1 3 3
1-T312-1 1 3 3
1-T321-1 1 3 3
1-T320-1 3 1 1
1-T322-1 1 5 6
1-T323-1 1 5 6
1-T324-1 1 3 3

Figure 33.



Open Tool Set
Ambiguity Group Number B1-2
Ambiguity Group Size 1
Cfg-Item Aspect
Item/Aspect Description
Cost to Replace
Time to Replace
Failure Probability
1-I310 -1
BLOCK "D"
BLOCK "D" Asp-1
++ 375.00
++ 30.00
++ 0.05347594
TOTALS
375.00
30.00
0.05347594
I300-1
L
I305-1
I301-3
T309-1
T311-1
F
I312-1
T313-1
E
I311-1
T312-1
D
I310-1
I302-1
W
T305-1
T325-1
T320-1
Diagnostic Flow Table
1-T307-1
1
Page 17
0
Good
Bad
Goto 1-T309-1
See Ambiguity Group
Diagnostic Flow Ta
Cfg-Test-Aspect
AG Size
Unique Quantity
Total QTY
1-T313-1 1 3 3
1-T311-1 1 3 3
1-T312-1 1 3 3
1-T321-1 1 3 3
1-T320-1 3 1 1
1-T322-1 1 5 6
1-T323-1 1 5 6
1-T324-1 1 3 3

Figure 34.

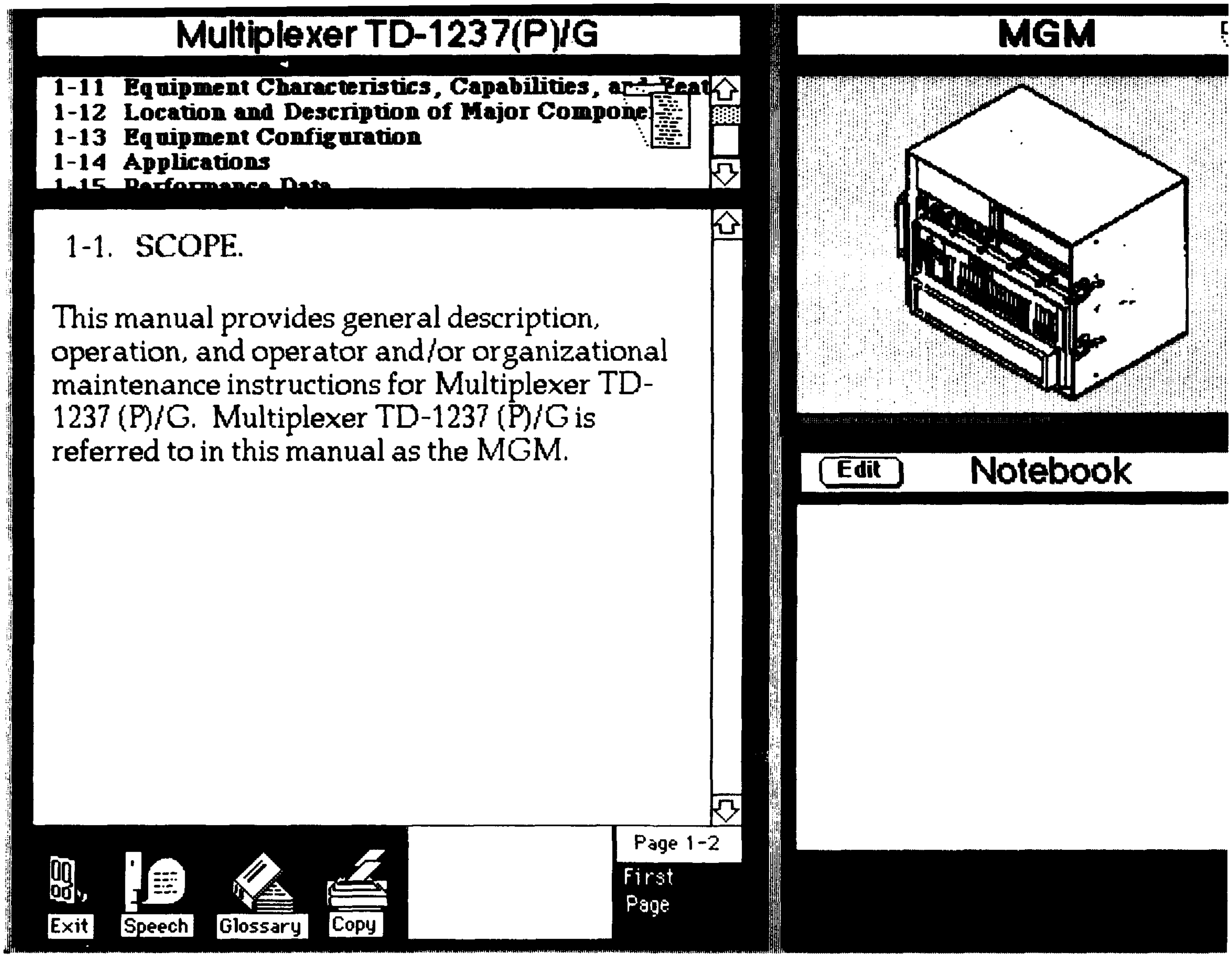

Multiplexer TD-1237(P)/G
1-11 Equipment Characteristics, Capabilities,
1-12 Location and Description of Major Compone
1-13 Equipment Configuration
1-14 Applications
1-1. SCOPE.
This manual provides general description, operation, and operator and/or organizational maintenance instructions for Multiplexer TD-1237 (P)/G. Multiplexer TD-1237 (P)/G is referred to in this manual as the MGM.
Page 1-2
First Page
Exit
Speech
Glossary
Copy
MGM
Edit
Notebook

Figure 35

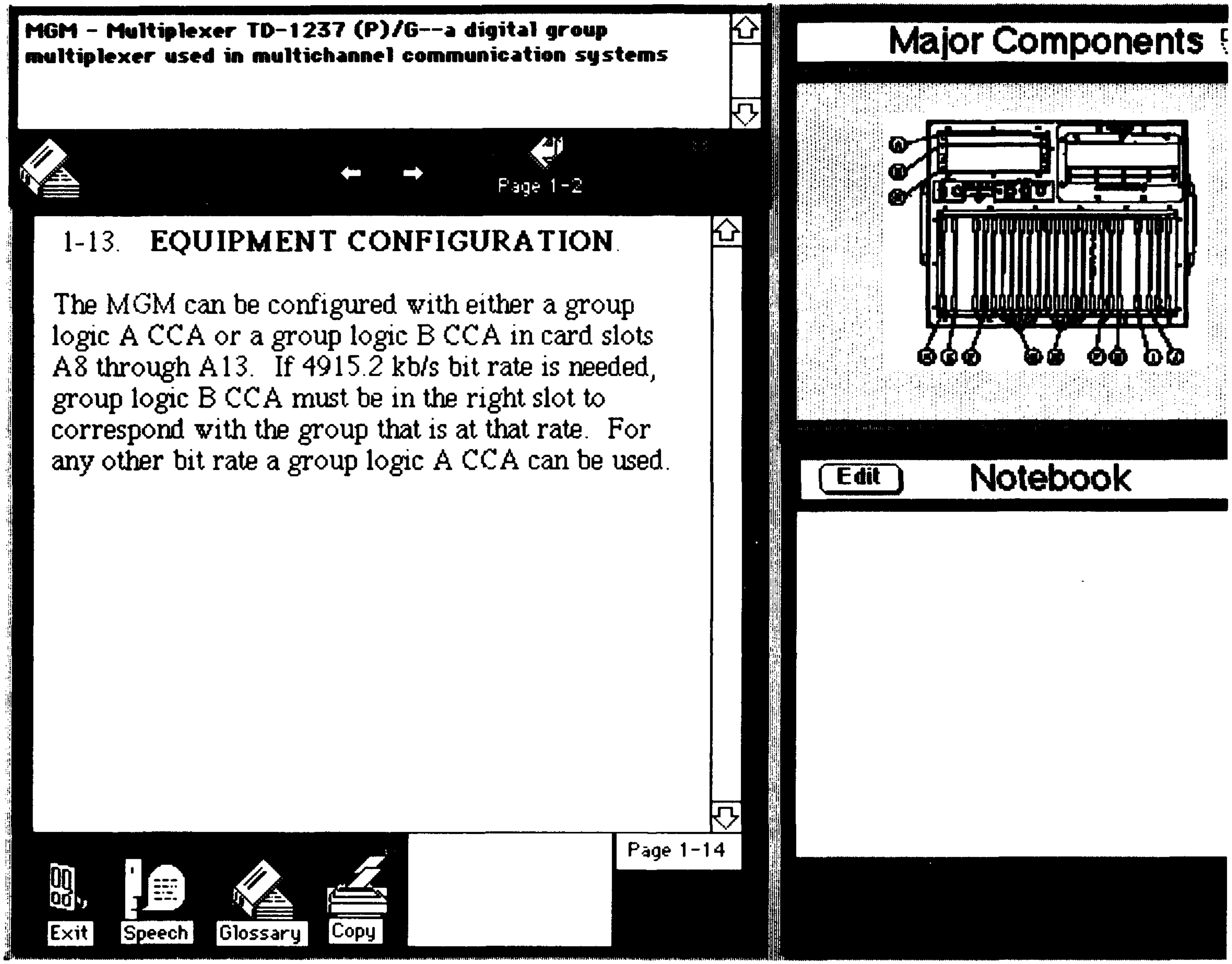

MGM - Multiplexer TD-1237 (P)/G--a digital group multiplexer used in multichannel communication systems
Page 1-2
1-13. EQUIPMENT CONFIGURATION.
The MGM can be configured with either a group logic A CCA or a group logic B CCA in card slots A8 through A13. If 4915.2 kb/s bit rate is needed, group logic B CCA must be in the right slot to correspond with the group that is at that rate. For any other bit rate a group logic A CCA can be used.
Page 1-14
Exit
Speech
Glossary
Copy
Major Components
Edit
Notebook

Figure 36

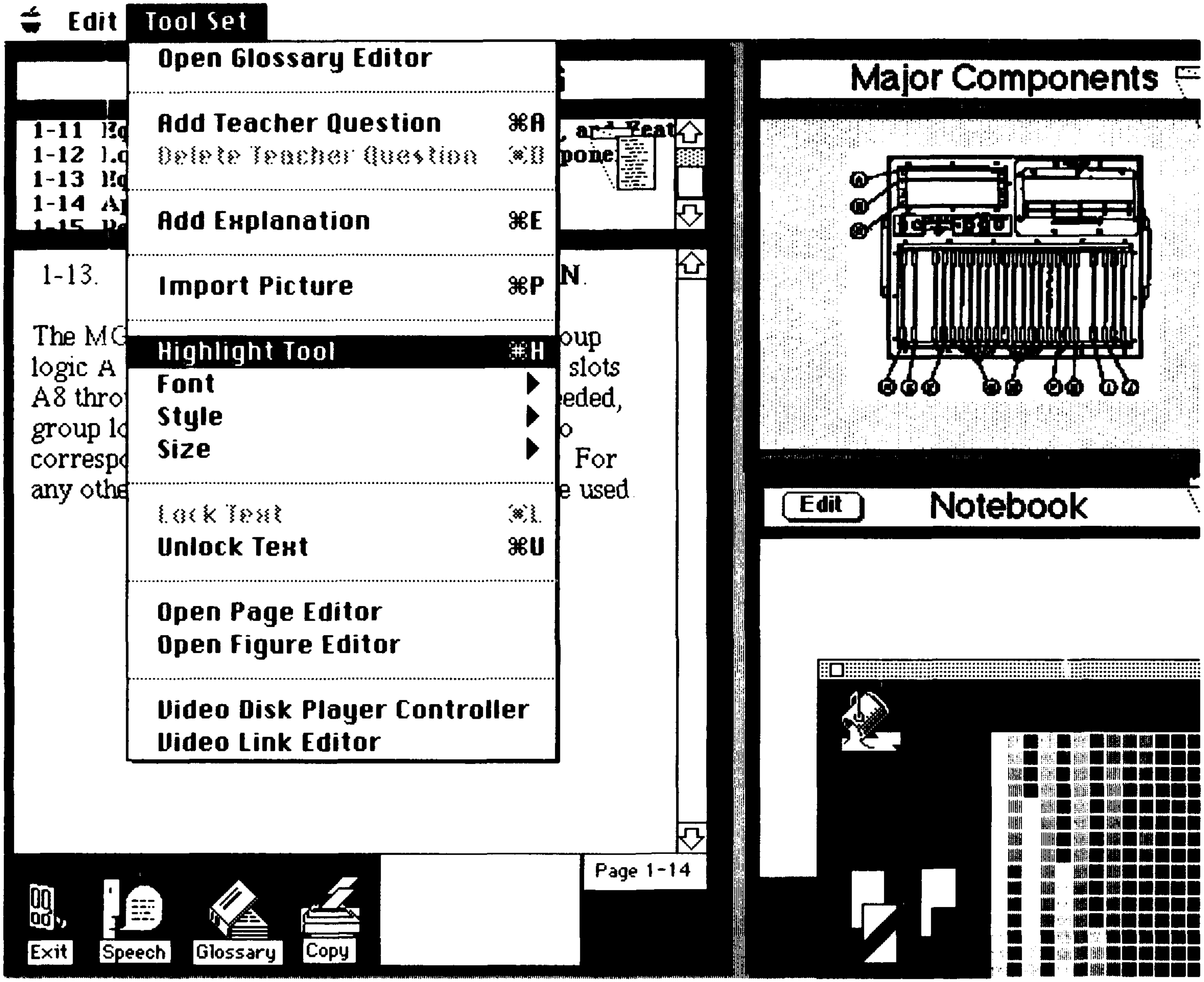
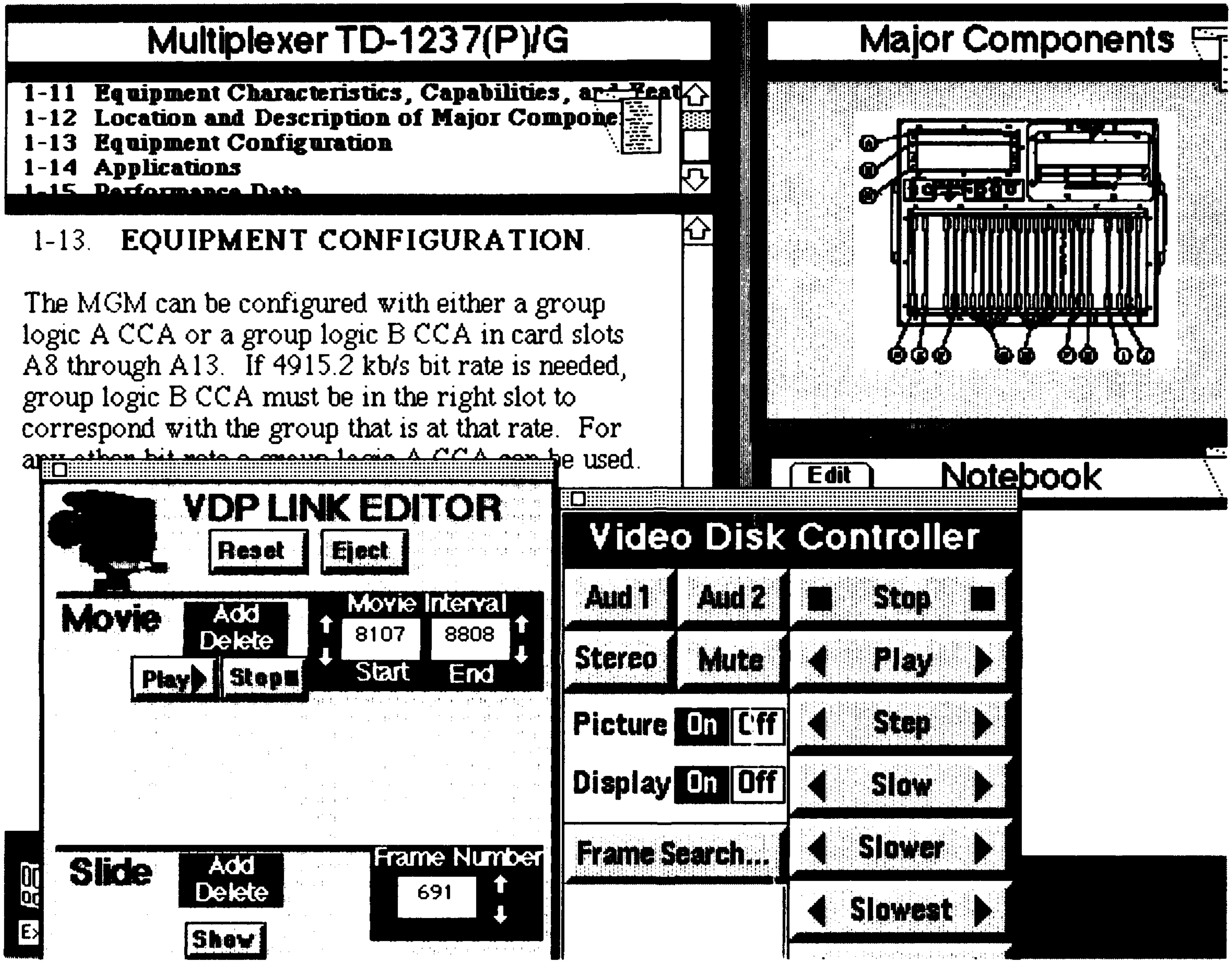

Edit
Tool Set
Open Glossary Editor
Add Teacher Question ⌘A
Delete Teacher Question ⌘D
Add Explanation ⌘E
Import Picture ⌘P
Highlight Tool ⌘H
Font
Style
Size
Lock Text ⌘L
Unlock Text ⌘U
Open Page Editor
Open Figure Editor
Video Disk Player Controller
Video Link Editor
Major Components
Edit
Notebook
Page 1-14
Exit
Speech
Glossary
Copy

Figure 37

72

73



Multiplexer TD-1237(P)/G
1-11 Equipment Characteristics, Capabilities,
1-12 Location and Description of Major Compone
1-13 Equipment Configuration
1-14 Applications
1-13. EQUIPMENT CONFIGURATION
The MGM can be configured with either a group logic A CCA or a group logic B CCA in card slots A8 through A13. If 4915.2 kb/s bit rate is needed, group logic B CCA must be in the right slot to correspond with the group that is at that rate. For
be used.
Major Components
Edit
Notebook
VDP LINK EDITOR
Reset
Eject
Movie
Add
Delete
Movie Interval
8107
8808
Start
End
Play
Stop
Slide
Add
Delete
Frame Number
691
Show
Video Disk Controller
Aud 1
Aud 2
Stop
Stereo
Mute
Play
Picture
On
Off
Step
Display
On
Off
Slow
Frame Search...
Slower
Slowest

Figure 38

Figure 4. Delinking Feeder

Go Instructions

Open Note Book

LEGEND

1. PUSH ROD GUIDE, FEEDER GEAR, AND STRIPPER SLEVE ASSE
2. ENTRANCE GUIDE
3. MACHINE SCREW
4. LINK GUIDE
5. FEEDER HOUSING

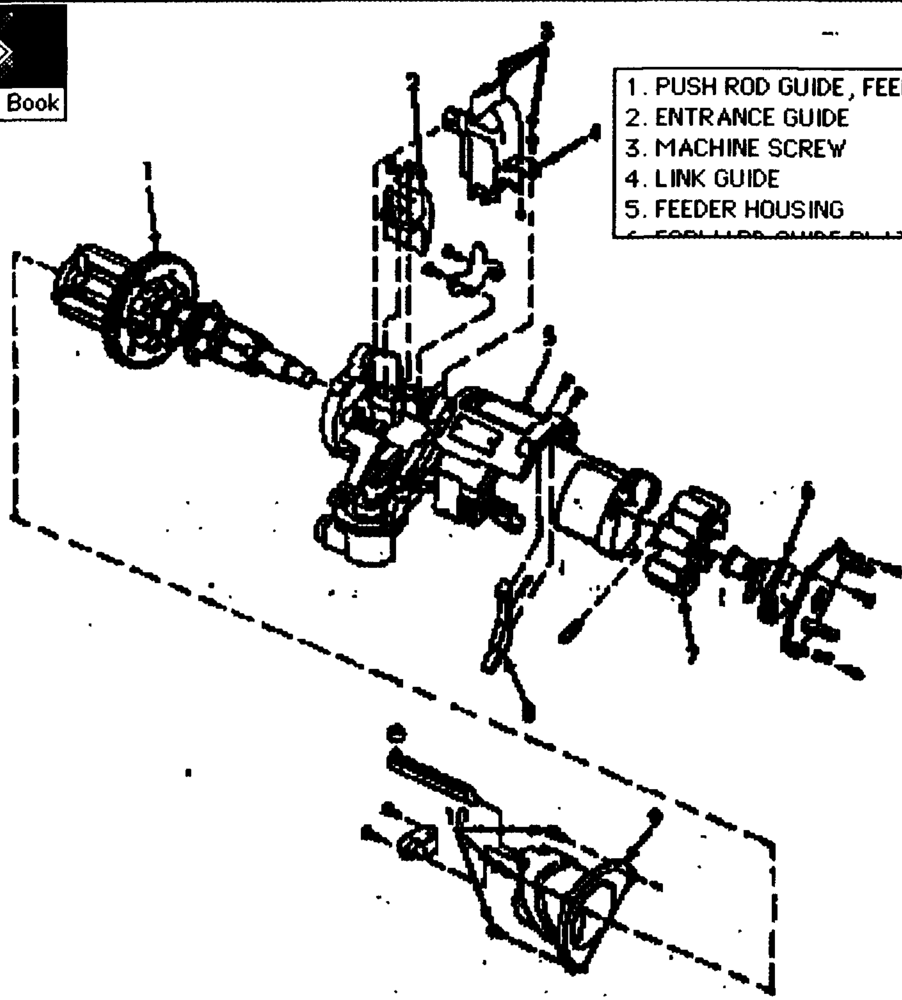


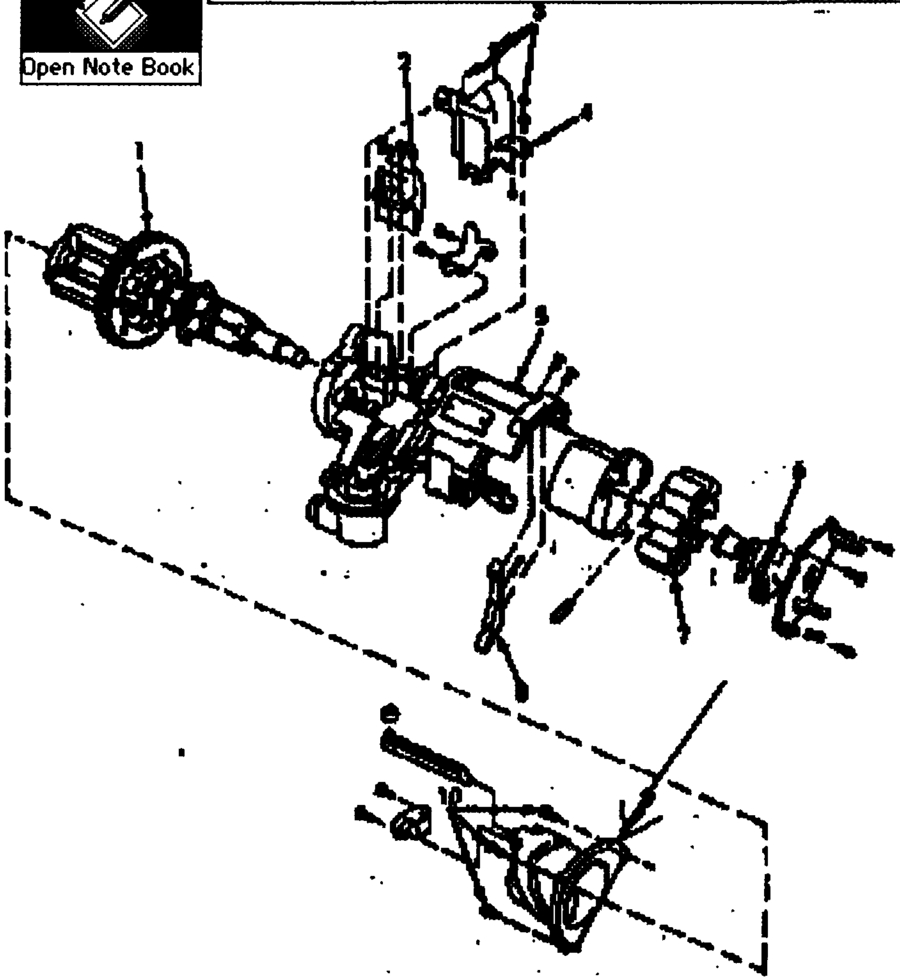
Figure 39

74

Whole Picture

Open Note Book

5. Remove rounds from feed sprocket, if neccessary remove feed guide.
If feeder is still jammed, proceed to step 6
6. Remove three screws securing cam housing assembly to feder housing
7. Retain push rod guide, feeder gear, and strepper sleeve assembly in cam housing assembly and carefuly separate cam housing assembly from feeder housing



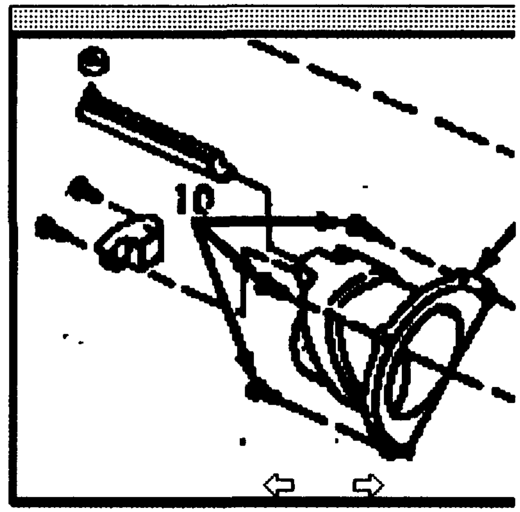


Figure 40

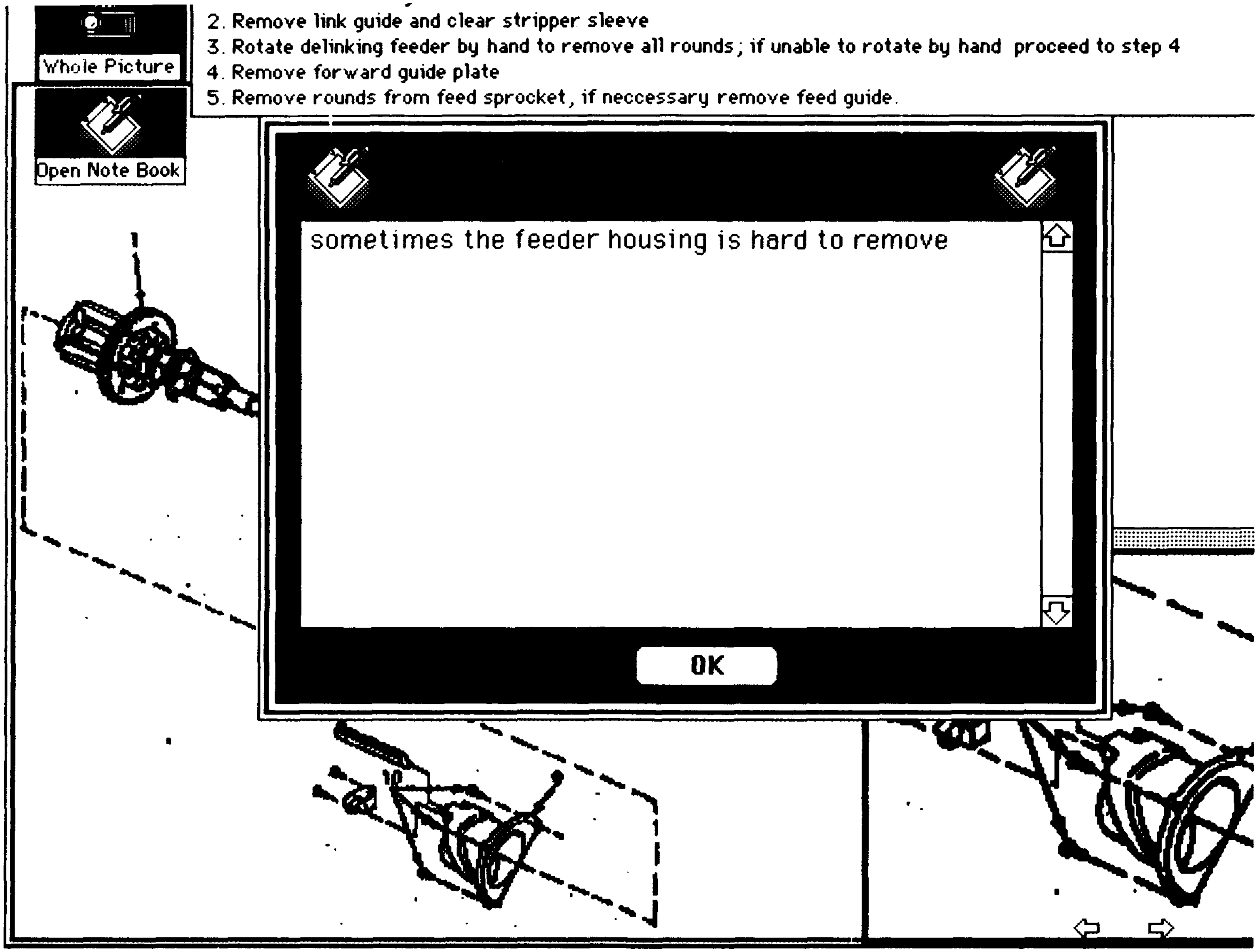

Whole Picture
Open Note Book
2. Remove link guide and clear stripper sleeve
3. Rotate delinking feeder by hand to remove all rounds; if unable to rotate by hand proceed to step 4
4. Remove forward guide plate
5. Remove rounds from feed sprocket, if neccessary remove feed guide.
sometimes the feeder housing is hard to remove
OK

Figure 41

Test Strategy Informaton Interchange Standard

Presentation to

SCC-20

October 29, 1990
Fort Lauderdale, Florida

by : Dr. Leonard S. Haynes
Intelligent Automation, Inc.
1370 Piccard Drive, Suite 210
Rockville, MD 20850
301-990-2407

Figure 42

IEEE

IEEE Standards
PROJECT AUTHORIZATION REQUEST (PAR)

1. Date of Request: Oct. 29, 1990 **2. Assigned Project #:**

---

3. Does this PAR revise a previously approved PAR? ☐ YES ☒ NO

---

4. Description of Proposed Document:

Standard	☐	New	☒	Trial Use	☒
Recommended Practice	☐	Revision	☐ of Std. ________	Full Use	☐
Guide	☐				

---

5. Project Title:

Test strategy information interchange standard

---

6. Scope of Proposed Standard: *(Use attachment sheet if necessary.)*

To define information interchange formats for the data required to characterize system component dependencies, failure rates, test times and reliabilities, ambiguity and test groups, diagnostic flowcharts, and directly related data.

---

7. Purpose of Proposed Standard: *(Use attachment sheet if necessary.)*

The proposed standard will allow tools related to testability analysis, test strategy and test sequence generation, maintenance aids and documentation, and life cycle cost prediction to share critical information.

---

8. SPONSOR: Society:

Committee: SCC-20

---

9. Name of group that will write the standard: SCC-20 Subcommittee on Test Strategy Information Interchange

10. Target Completion Date: 6/93

---

11. Proposed Coordination: *(See instructions.)*

	Method of Coordination:
SCC10 (IEEE Dictionary)	
Robotics and Automation Society	Liaison Member
Industrial Electronics Society	Circulation of Draft
ASC X3	Circulation of Draft
DASS	Circulation of Draft

---

12. Are you aware of any patent, copyright, or trademark issues? ☐ YES ☒ NO
(If yes, attach a sheet with an explanation.)

Are you aware of any standards or projects with a similiar scope? ☐ YES ☒ NO
(If yes, attach a sheet with a complete description of the impact of the similarities.)

Figure 43

PROJECT AUTHORIZATION REQUEST (PAR)
(cont'd)

13. Copyright Agreement for IEEE Standards

I hereby acknowledge my appointment as Official Reporter to the ____________________ Committee to write/revise a Standards Publication (entitled or to be entitled)____________________

____

In consideration of my appointment and the publication of the Standards Publication identifying me, at my option, as an Official Reporter, I agree to avoid knowingly incorporating in the Standards Publication any copyrighted or proprietary material of another without such other's consent and acknowledge that the Standards Publication shall constitute a "work made for hire" as defined by the Copyright Act, and, that as to any work not so defined, I agree to and do hereby transfer any right or interest I may have in the copyright to said Standards Publication to IEEE.

Name____________________
(signature of chair of working group)

Title____________________

Date October 29, 1990

14. Person delegated to receive communications and conduct liaison with interested bodies:
(This is normally the chair of the working group. If not, please indicate IEEE position.)

Name Leonard S. Haynes
Telephone 301-990-2407
Company Intelligent Automation, Inc.
Fax 301-990-2409
Address 1370 Piccard Drive, Suite 210
Telex____________________
City Rockville, State MD
Zip 20850 E Mail____________________

15. Submitted By:
(This is normally the sponsor's liaison to the Standards Board . If not, please indicate IEEE position and relationship to the sponsor.)

Name____________________
Telephone____________________
Company____________________
Fax____________________
Address____________________
Telex____________________
City____________________ State____________________
Zip____________ E Mail____________________

APPENDIX 1

OUTPUT FROM STAT DEPENDENCY-BASED TESTABILITY TOOL MARKETED BY DETEX SYSTEMS, INCORPORATED

DATA FROM ROBOTIC HAND-EYE COORDINATION SYSTEM - HIGH LEVEL SYSTEM BLOCK DIAGRAM LEVEL

THE ROBOTIC HAND-EYE COORDINATION SYSTEM WAS DEVELOPED BY IAI FOR THE ARMY ARMAMENT RESEARCH, DEVELOPMENT, AND ENGINEERING CENTER, PICATINNY ARSENAL, NJ

1. T1-1:

Description : camera1_input
Cost of Test : 0.00
Time to Test : 0.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

2. T2-2:

Description : camera2_input
Cost of Test : 0.00
Time to Test : 0.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

3. T3-1:

Description : test_data_input
Cost of Test : 0.00
Time to Test : 0.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

4. T4-1:

Description : test_image1
Cost of Test : 2.00
Time to Test : 2.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I1-1

o Cause Test Dependencies:
To Item Aspect I1-1: [1]
T1-1

5. T5-1:

Description : test_image2
Cost of Test : 2.00
Time to Test : 2.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I2-1

o Cause Test Dependencies:
To Item Aspect I2-1: [1]
T2-1

6. T2-1:

Description : camera2_input
Cost of Test : 0.00
Time to Test : 0.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

7. T6-1:

Description : check_claibration
Cost of Test : 4.00
Time to Test : 4.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I3-1

o Cause Test Dependencies:
To Item Aspect I3-1: [1]
T3-1

8. T7-1:

Description : grab_frame_signal
Cost of Test : 3.00
Time to Test : 3.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I10-1

o Cause Test Dependencies:
To Item Aspect I10-1: [1]
T13-1

9. T13-1:

Description : sync_signal
Cost of Test : 2.00
Time to Test : 2.00 minute(s)
Enclosure # : 1
Level # : 1

```
                    Type              : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I9-1

        o Cause Test Dependencies:
         To Item Aspect I9-1: [1]
            T12-1


 10.   T8-1:
                    Description       : composite_image
                    Cost of Test      : 2.00
                    Time to Test      : 2.00 minute(s)
                    Enclosure #       : 1
                    Level #           : 1
                    Type              : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I4-1

        o Cause Test Dependencies:
         To Item Aspect I4-1: [3]
            T4-1          T5-1          T7-1


 11.   T9-1:
                    Description       : 3-D point
                    Cost of Test      : 3.00
                    Time to Test      : 3.00 minute(s)
                    Enclosure #       : 1
                    Level #           : 1
                    Type              : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I5-1

        o Cause Test Dependencies:
         To Item Aspect I5-1: [1]
            T8-1 , T6-1


 12.   T10-1:
                    Description       : trajectory
                    Cost of Test      : 1.00
                    Time to Test      : 1.00 minute(s)
                    Enclosure #       : 1
                    Level #           : 1
                    Type              : PROBE
                    Selection Status: ALLOWED
```

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I6-1

o Cause Test Dependencies:
To Item Aspect I6-1: [1]
T9-1

13. T11-1:

Description	:	smooth_path
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I7-1

o Cause Test Dependencies:
To Item Aspect I7-1: [1]
T10-1

14. T12-1:

Description	:	robot_control_signs
Cost of Test	:	4.00
Time to Test	:	4.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I8-1

o Cause Test Dependencies:
To Item Aspect I8-1: [2]
T11-1 T14-1

15. T14-1:

Description	:	command_to_robot
Cost of Test	:	5.00
Time to Test	:	5.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [2]

1. I1:

Description : camera1
Cost to Replace : 1200.00
Time to Replace : 1.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

2. I2:

Description : camera2
Cost to Replace : 1200.00
Time to Replace : 1.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

3. I3:

Description : camera_calibration
Cost to Replace : 100.00
Time to Replace : 30.00 minute(s)
Failure Rate : 0.00100000
Aspect Descriptions:
1. <NONE>

4. I10:

Description : control
Cost to Replace : 500.00
Time to Replace : 10.00 minute(s)
Failure Rate : 0.00005000
Aspect Descriptions:
1. <NONE>

5. I4:

Description : image_frame_grabber
Cost to Replace : 1500.00
Time to Replace : 30.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

6. I5:

Description : 2D_to_3D_conv
Cost to Replace : 400.00
Time to Replace : 20.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

7. I6:

Description : traj_predictor
Cost to Replace : 500.00
Time to Replace : 30.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

8. I7:

Description : smoothing_board
Cost to Replace : 500.00
Time to Replace : 30.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

```
9.    I8:
              Description      : robot_control
              Cost to Replace  : 500.00
              Time to Replace  : 30.00 minute(s)
              Failure Rate     : 0.00010000
              Aspect Descriptions:
                  1. <NONE>

10.   I9:
              Description      : robot_control_port
              Cost to Replace  : 250.00
              Time to Replace  : 60.00 minute(s)
              Failure Rate     : 0.00050000
              Aspect Descriptions:
                  1. <NONE>
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
 ________________________________        ______________________________
|  1-T15   -1                    |      |                              |
|robot_output                    |      |  NO FAULTS ENCOUNTERED       |
|                                |      |                              |
|                                |      |                              |
|weighting   :+0.00000000        |  G   |cumulative totals             |
|                                |------|      tests:      1           |
|time so far:          0.00      |      |  test cost:          1.00    |
|cost to go :       4159.00      |      |  test time:          1.00    |
|time to go :        219.00      |      | enclosures:      1           |
|________________________________|      |______________________________|
 _______________B|_______________
|  1-T6    -1                    |
|check_claibration               |
|                                |
|                                |
|weighting   :+0.00000000        |  G
|                                |---------------------------------------
|time so far:          1.00      |                                 to page
|cost to go :       4158.00      |                                   0010
|time to go :        218.00      |                                   1-T5
|________________________________|                                     -1
 _______________B|_______________        ______________________________
|  1-T3    -1                    |      |   ****** FAULT ******        |
|test_data_input                 |      |                              |
|                                |      |Sus AG Ref#:      1           |
|                                |      |                              |
|weighting   :+0.00000000        |  G   |cumulative totals             |
|                                |------|      tests:      3           |
|time so far:          5.00      |      |  test cost:          5.00    |
|cost to go :        100.00      |      |  test time:          5.00    |
|time to go :         30.00      |      | enclosures:      1           |
|________________________________|      |______________________________|
 _______________B|_______________
|  ****** FAULT ******           |
|                                |
|  Input :   1-T3    -1          |
|                                |
|cumulative totals               |
|      tests:      3             |
|  test cost:          5.00      |
|  test time:          5.00      |
| enclosures:      1             |
|________________________________|
```

SYSTEM   8: trypipe1
MODEL   2: model2   CASE   1: 1

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
              _________________________
             |  1-T5    -1             |
             |test_image2              |
             |                         |
             |                         |
     G       |weighting  :+0.00000000  | G
-------------|                         |----------------------------------------
from page    |time so far:        5.00 |                                 to page
  0009       |cost to go :     4154.00 |                                   0011
  1-T6       |time to go :      214.00 |                                   1-T4
    -1       |_________________________|                                     -1
              ____________B|___________     _________________________
             |  1-T2    -1             |   |  ****** FAULT ******    |
             |camera2_input            |   |                         |
             |                         |   |Sus AG Ref#:      2      |
             |                         |   |                         |
             |weighting  :+0.00000000  | G |cumulative totals        |
             |                         |---|      tests:      4      |
             |time so far:        7.00 |   |  test cost:         7.00|
             |cost to go :     1200.00 |   |  test time:         7.00|
             |time to go :        1.00 |   | enclosures:      1      |
             |_________________________|   |_________________________|
              ____________B|___________
             |  ****** FAULT ******    |
             |                         |
             |  Input :   1-T2    -1   |
             |                         |
             |cumulative totals        |
             |      tests:      4      |
             |  test cost:        7.00 |
             |  test time:        7.00 |
             | enclosures:      1      |
             |_________________________|
```

SYSTEM   8: trypipe1
MODEL   2: model2   CASE   1: 1

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
             _________________________        _________________________
            |  1-T4    -1             |      |   ****** FAULT ******   |
            |test_image1              |      |                         |
            |                         |      |Sus AG Ref#:     4       |
            |                         |      |                         |
    G       |weighting  :+0.00000000  |  G   |cumulative totals        |
------------|                         |------|      tests:     4       |
from page   |time so far:         7.00|      | test cost:         9.00 |
  0010      |cost to go :      4152.00|      | test time:         9.00 |
  1-T5      |time to go :       212.00|      | enclosures:      1      |
   -1       |_________________________|      |_________________________|
             ___________B|_____________       _________________________
            |  1-T1    -1             |      |   ****** FAULT ******   |
            |camera1_input            |      |                         |
            |                         |      |Sus AG Ref#:     3       |
            |                         |      |                         |
            |weighting  :+0.00000000  |  G   |cumulative totals        |
            |                         |------|      tests:     5       |
            |time so far:         9.00|      | test cost:         9.00 |
            |cost to go :      1200.00|      | test time:         9.00 |
            |time to go :         1.00|      | enclosures:      1      |
            |_________________________|      |_________________________|
             ___________B|_____________
            |  ****** FAULT ******    |
            |                         |
            |  Input :   1-T1    -1   |
            |                         |
            |cumulative totals        |
            |      tests:     5       |
            | test cost:         9.00 |
            | test time:         9.00 |
            | enclosures:      1      |
            |_________________________|
```

APPENDIX 2

OUTPUT FROM STAT DEPENDENCY-BASED TESTABILITY TOOL MARKETED BY DETEX SYSTEMS, INCORPORATED

DATA FROM INTERLACED/NON-INTERLACED SYNC SIGNAL GENERATION DETAILED CIRCUIT DIAGRAM

THE INTERLACED/NON-INTERLACED SYNC SIGNAL GENERATION CIRCUIT WAS PRODUCED BY IAI FOR THE ARMY ARMAMENT RESEARCH, DEVELOPMENT, AND ENGINEERING CENTER, PICATINNY ARSENAL, NJ.

1. T1-1:

```
Description      : VSYNC input
Cost of Test     : 1.00
Time to Test     : 1.00 minute(s)
Enclosure #      : 1
Level #          : 1
Type             : PROBE
Selection Status: ALLOWED
```

2. T2-1:

```
Description      : digitized VSYNC
Cost of Test     : 1.00
Time to Test     : 1.00 minute(s)
Enclosure #      : 1
Level #          : 1
Type             : PROBE
Selection Status: ALLOWED
```

```
o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
    I1-1

o Cause Test Dependencies:
  To Item Aspect I1-1: [1]
    T1-1
```

3. T3-1:

```
Description      : VNORM inverse
Cost of Test     : 1.00
Time to Test     : 1.00 minute(s)
Enclosure #      : 1
Level #          : 1
Type             : PROBE
Selection Status: ALLOWED
```

```
o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
    I2-1

o Cause Test Dependencies:
  To Item Aspect I2-1: [1]
    T2-1
```

4. T7-1:

```
Description      : 4 us pulse @ VSYNC
Cost of Test     : 4.00
Time to Test     : 4.00 minute(s)
Enclosure #      : 1
Level #          : 1
Type             : PROBE
Selection Status: ALLOWED
```

```
o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
    I3-1
```

o Cause Test Dependencies:
To Item Aspect I3-1: [1]
T3-1

5. T4-1:

Description	:	HSYNC input
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies:

o Cause Test Dependencies:
To Item Aspect

6. T5-1:

Description	:	digitived HSYNC
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I5-1

o Cause Test Dependencies:
To Item Aspect I5-1: [1]
T4-1

7. T6-1:

Description	:	HNORM inverse
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I6-1

o Cause Test Dependencies:
To Item Aspect I6-1: [1]

T5-1

8. T8-1:

Description	:	ODD inverse pulse
Cost of Test	:	4.00
Time to Test	:	4.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

- o Dangling Tests: [0]
- o Item Aspect Dependencies: [1]
  I4-1
- o Cause Test Dependencies:
  To Item Aspect I4-1: [2]
  T7-1 T6-1

9. T9-1:

Description	:	<NONE>
Cost of Test	:	0.00
Time to Test	:	0.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

- o Dangling Tests: [0]
- o Item Aspect Dependencies: [1]
- o Cause Test Dependencies:
  To Item Aspect [1]

10. T10-1:

Description	:	x100 counter out
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

- o Dangling Tests: [0]
- o Item Aspect Dependencies: [1]
  I8-1
- o Cause Test Dependencies:
  To Item Aspect I8-1: [2]
  T8-1 T13-1

11. T13-1:

Description : x100 ripple in
Cost of Test : 1.00
Time to Test : 1.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I9-1

o Cause Test Dependencies:
To Item Aspect I9-1: [2]
T8-1 T14-1

12. T11-1:

Description : x10 counter out
Cost of Test : 1.00
Time to Test : 1.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I9-1

o Cause Test Dependencies:
To Item Aspect I9-1: [2]
T8-1 T14-1

13. T14-1:

Description : x 10 ripple in
Cost of Test : 1.00
Time to Test : 1.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I10-1

o Cause Test Dependencies:
To Item Aspect I10-1: [2]
T8-1 T15-1

14. T12-1:

Description : x1 counter out

Cost of Test : 1.00
Time to Test : 1.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I10-1

o Cause Test Dependencies:
To Item Aspect I10-1: [2]
T8-1 T15-1

15. T15-1:

Description : x1 counter out
Cost of Test : 1.00
Time to Test : 1.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I7-1

o Cause Test Dependencies:
To Item Aspect I7-1: [1]
T6-1

16. T16-1:

Description : count 262 pulse out
Cost of Test : 4.00
Time to Test : 4.00 minute(s)
Enclosure # : 1
Level # : 1
Type : PROBE
Selection Status: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I11-1

o Cause Test Dependencies:
To Item Aspect I11-1: [3]
T10-1 T11-1 T12-1

17. T17-1:

Description : count 262 pulse
Cost of Test : 4.00
Time to Test : 4.00 minute(s)
Enclosure # : 1

```
                    Level #          : 1
                    Type             : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I12-1

        o Cause Test Dependencies:
         To Item Aspect I12-1: [1]
            T16-1


18.   T18-1:
                    Description      : count 9 HSYNC pulse
                    Cost of Test     : 2.00
                    Time to Test     : 2.00 minute(s)
                    Enclosure #      : 1
                    Level #          : 1
                    Type             : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I13-1

        o Cause Test Dependencies:
         To Item Aspect I13-1: [1]
            T17-1


19.   T19-1:
                    Description      : VFAKE inverse
                    Cost of Test     : 1.00
                    Time to Test     : 1.00 minute(s)
                    Enclosure #      : 1
                    Level #          : 1
                    Type             : PROBE
                    Selection Status: ALLOWED

        o Dangling Tests: [0]

        o Item Aspect Dependencies: [1]
            I14-1

        o Cause Test Dependencies:
         To Item Aspect I14-1: [2]
            T18-1          T17-1


20.   T20-1:
                    Description      : VFAKE & non-intrl
                    Cost of Test     : 1.00
                    Time to Test     : 1.00 minute(s)
                    Enclosure #      : 1
                    Level #          : 1
                    Type             : PROBE
                    Selection Status: ALLOWED
```

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I16-1

o Cause Test Dependencies:
To Item Aspect I16-1: [2]
T19-1 T25-1

21. T25-1:

Description	: non-intr mode
Cost of Test	: 1.00
Time to Test	: 1.00 minute(s)
Enclosure #	: 1
Level #	: 1
Type	: PROBE
Selection Status	: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I18-1

o Cause Test Dependencies:
To Item Aspect I18-1: [2]
T21-1 T23-1

22. T21-1:

Description	: VNORM & interl
Cost of Test	: 1.00
Time to Test	: 1.00 minute(s)
Enclosure #	: 1
Level #	: 1
Type	: PROBE
Selection Status	: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I15-1

o Cause Test Dependencies:
To Item Aspect I15-1: [2]
T3-1 T24-1

23. T24-1:

Description	: interlace mode
Cost of Test	: 1.00
Time to Test	: 1.00 minute(s)
Enclosure #	: 1
Level #	: 1
Type	: PROBE
Selection Status	: ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I18-1

o Cause Test Dependencies:
To Item Aspect I18-1: [2]
T21-1 T23-1

24. T22-1:

Description	:	select mode input
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

25. T23-1:

Description	:	ODD inv & mode sel
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I19-1

o Cause Test Dependencies:
To Item Aspect I19-1: [2]
T8-1 T22-1

26. T26-1:

Description	:	VSYNC input
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)
Enclosure #	:	1
Level #	:	1
Type	:	PROBE
Selection Status	:	ALLOWED

o Dangling Tests: [0]

o Item Aspect Dependencies: [1]
I17-1

o Cause Test Dependencies:
To Item Aspect I17-1: [2]
T21-1 T20-1

27. T27-1:

Description	:	HNEW inverse out
Cost of Test	:	1.00
Time to Test	:	1.00 minute(s)

```
      I10-1        I1-1

  o Cause Test Dependencies:
   To Item Aspect I10-1: [1]
      T13-1


16.   T15-1:
                 Description      : robot_output
                 Cost of Test     : 1.00
                 Time to Test     : 1.00 minute(s)
                 Enclosure #      : 1
                 Level #          : 1
                 Type             : PROBE
                 Selection Status : ALLOWED

  o Dangling Tests: [0]

  o Item Aspect Dependencies: [1]
      I9-1

  o Cause Test Dependencies:
   To Item Aspect I9-1: [1]
      T12-1
```

```
                     Enclosure #      : 1
                     Level #          : 1
                     Type             : PROBE
                     Selection Status: ALLOWED

          o Dangling Tests: [0]

          o Item Aspect Dependencies: [2]
               I20-1

          o Cause Test Dependencies:
            To Item Aspect I20-1: [1]
               T6-1


28.    T2-2:
                     Description      : <NONE>
                     Cost of Test     : 0.00
                     Time to Test     : 0.00 minute(s)
                     Enclosure #      : 1
                     Level #          : 1
                     Type             : PROBE
                     Selection Status: ALLOWED
```

1. I1:

Description : VSYNC input op amp
Cost to Replace : 2.00
Time to Replace : 1000.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

2. I2:

Description : inverter
Cost to Replace : 1.00
Time to Replace : 10.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

3. I3:

Description : 4 um one shot
Cost to Replace : 2.00
Time to Replace : 10.00 minute(s)
Failure Rate : 0.00005000
Aspect Descriptions:
1. <NONE>

4. I5:

Description : HSYNC op amp
Cost to Replace : 2.00
Time to Replace : 10.00 minute(s)
Failure Rate : 0.00010000
Aspect Descriptions:
1. <NONE>

5. I6:

Description : HSYNC inverter
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

6. I4:

Description : 2 input or gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

7. I7:

Description : inverter
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

8. I8:

Description : x10 counter
Cost to Replace : 3.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

9. I9:

Description : x10 counter
Cost to Replace : 2.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

10. I10:

Description : x10 counter
Cost to Replace : 2.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

11. I11:

Description : 3 input and gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00001000
Aspect Descriptions:
1. <NONE>

12. I12:

Description : 4 us one shot
Cost to Replace : 4.00
Time to Replace : 3.00 minute(s)
Failure Rate : 0.00005000
Aspect Descriptions:
1. <NONE>

13. I13:

Description : x10 counter
Cost to Replace : 2.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00002000
Aspect Descriptions:
1. <NONE>

14. I14:

Description : flip flop
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00001000
Aspect Descriptions:
1. <NONE>

15. I16:

Description : 2 input or gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00000500
Aspect Descriptions:
1. <NONE>

16. I15:

Description : 2 input or gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate : 0.00000200
Aspect Descriptions:

1. <NONE>

17. I19:

```
Description     : 2 input and gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate    : 0.00000200
Aspect Descriptions:
    1. <NONE>
```

18. I18:

```
Description     : flip flop
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate    : 0.00000200
Aspect Descriptions:
    1. <NONE>
```

19. I17:

```
Description     : 2 input and gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate    : 0.00000200
Aspect Descriptions:
    1. <NONE>
```

20. I20:

```
Description     : 2 input and gate
Cost to Replace : 1.00
Time to Replace : 2.00 minute(s)
Failure Rate    : 0.00000200
Aspect Descriptions:
    1. <NONE>
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS   Diagnostic Flow Diagram

```
 ______________________________
| 1-T26  -1                    |
|VSYNC input                   |
|                              |
|                              |
|weighting  :+0.00000000       | G
|                              |---------------------------------------
|time so far:        0.00      |                                 to page
|cost to go :       17.00      |                                  0019
|time to go :       23.00      |                                  1-T27
|______________________________|                                    -1
 _____________B|______________
| 1-T25  -1                    |
|non-intr mode                 |
|                              |
|                              |
|weighting  :+0.00000000       | G
|                              |---------------------------------------
|time so far:        1.00      |                                 to page
|cost to go :       16.00      |                                  0014
|time to go :       22.00      |                                  1-T16
|______________________________|                                    -1
 _____________B|______________
| 1-T8   -1                    |
|ODD inverse pulse             |
|                              |
|                              |
|weighting  :+0.00000000       | G
|                              |---------------------------------------
|time so far:        2.00      |                                 to page
|cost to go :       13.00      |                                  0013
|time to go :       21.00      |                                  1-T23
|______________________________|                                    -1
 _____________B|______________
| 1-T7   -1                    |
|4 us pulse @ VSYNC            |
|                              |
|                              |
|weighting  :+0.00000000       | G
|                              |---------------------------------------
|time so far:        6.00      |                                 to page
|cost to go :        9.00      |                                  0011
|time to go :       17.00      |                                  1-T6
|______________________________|                                    -1
 _____________B|______________     ______________________________
| 1-T3   -1                    |  |   ****** FAULT ******        |
|VNORM inverse                 |  |                              |
|                              |  |Sus AG Ref#:      3           |
|                              |  |                              |
|weighting  :+0.00000000       | G|cumulative totals             |
|                              |---|       tests:     5          |
|time so far:       10.00      |  |  test cost:       11.00      |
|cost to go :        5.00      |  |  test time:       11.00      |
|time to go :       12.00      |  | enclosures:       1          |
|______________________________|  |______________________________|
              B|
to page 0010   |    1-T0002-1
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
  from page |    1-T3
    0009    |     -1
 ___________B|____________      ______________________
|  1-T2    -1             |    |   ****** FAULT ******  |
|digitized VSYNC          |    |                        |
|                         |    |Sus AG Ref#:      2     |
|                         |    |                        |
|weighting  :+0.00000000  | G  |cumulative totals       |
|                         |---|      tests:       6     |
|time so far:      11.00  |    |  test cost:       12.00 |
|cost to go :       4.00  |    |  test time:       12.00 |
|time to go :      11.00  |    | enclosures:       1     |
|_________________________|    |________________________|
 ___________B|____________      ______________________
|  1-T1    -1             |    |   ****** FAULT ******  |
|VSYNC input              |    |                        |
|                         |    |Sus AG Ref#:      1     |
|                         |    |                        |
|weighting  :+0.00000000  | G  |cumulative totals       |
|                         |---|      tests:       7     |
|time so far:      12.00  |    |  test cost:       13.00 |
|cost to go :       3.00  |    |  test time:       13.00 |
|time to go :       6.00  |    | enclosures:       1     |
|_________________________|    |________________________|
 ___________B|____________
|  ****** FAULT ******     |
|                         |
|  Input :    1-T1    -1  |
|                         |
|cumulative totals        |
|      tests:      7      |
|  test cost:      13.00  |
|  test time:      13.00  |
| enclosures:      1      |
|_________________________|
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
              ________________________      ________________________
             | 1-T6   -1              |    |  ****** FAULT ******   |
             |HNORM inverse           |    |                        |
             |                        |    |Sus AG Ref#:     6      |
             |                        |    |                        |
     G       |weighting  :+0.00000000 | G  |cumulative totals       |
 ----------- |                        |----|      tests:     5      |
 from page   |time so far:      10.00 |    |  test cost:      11.00 |
   0009      |cost to go :       5.00 |    |  test time:      11.00 |
   1-T7      |time to go :      13.00 |    | enclosures:     1      |
     -1      |________________________|    |________________________|
              ____________B|____________    ________________________
             | 1-T5   -1              |    |  ****** FAULT ******   |
             |digitived HSYNC         |    |                        |
             |                        |    |Sus AG Ref#:     5      |
             |                        |    |                        |
             |weighting  :+0.00000000 | G  |cumulative totals       |
             |                        |----|      tests:     6      |
             |time so far:      11.00 |    |  test cost:      12.00 |
             |cost to go :       4.00 |    |  test time:      12.00 |
             |time to go :      12.00 |    | enclosures:     1      |
             |________________________|    |________________________|
                          B|
             to page 0012 |   1-T0004-1
```

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FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
   from page |    1-T5
     0011    |     -1
 ___________B|___________     ________________________
| 1-T4    -1            |   |  ****** FAULT ******     |
|HSYNC input            |   |                          |
|                       |   |Sus AG Ref#:     4        |
|                       |   |                          |
|weighting  :+0.00000000| G |cumulative totals         |
|                       |---|      tests:     7        |
|time so far:      12.00|   |  test cost:       13.00  |
|cost to go :       3.00|   |  test time:       13.00  |
|time to go :      11.00|   | enclosures:     1        |
|_______________________|   |__________________________|
 ___________B|___________
|  ****** FAULT ******  |
|                       |
|  Input :   1-T4   -1  |
|                       |
|cumulative totals      |
|      tests:     7     |
|  test cost:      13.00|
|  test time:      13.00|
| enclosures:     1     |
|_______________________|
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
               ________________________________    _____________________________
              | 1-T23  -1                     |   | ****** FAULT ******         |
              |ODD inv & mode sel             |   |                             |
              |                               |   |Sus AG Ref#:     8           |
              |                               |   |                             |
     G        |weighting  :+0.00000000        | G |cumulative totals            |
 -------------|                               |---|      tests:     4           |
 from page    |time so far:           6.00    |   | test cost:           7.00   |
   0009       |cost to go :           3.00    |   | test time:           7.00   |
   1-T8       |time to go :           5.00    |   | enclosures:     1           |
    -1        |_______________________________|   |_____________________________|
               _____________B|________________     _____________________________
              | 1-T22  -1                     |   | ****** FAULT ******         |
              |select mode input              |   |                             |
              |                               |   |Sus AG Ref#:     7           |
              |                               |   |                             |
              |weighting  :+0.00000000        | G |cumulative totals            |
              |                               |---|      tests:     5           |
              |time so far:           7.00    |   | test cost:           8.00   |
              |cost to go :           2.00    |   | test time:           8.00   |
              |time to go :           3.00    |   | enclosures:     1           |
              |_______________________________|   |_____________________________|
               _____________B|________________
              | ****** FAULT ******           |
              |                               |
              | Input :   1-T22  -1           |
              |                               |
              |cumulative totals              |
              |      tests:     5             |
              | test cost:            8.00    |
              | test time:            8.00    |
              | enclosures:     1             |
              |_______________________________|
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
                 _____________________________
                | 1-T16  -1                   |
                |count 262 pulse out          |
                |                             |
                |                             |
     G          |weighting  :+0.00000000      | G
 ---------------|                             |----------------------------------------
 from page      |time so far:         2.00    |                                 to page
   0009         |cost to go :        15.00    |                                  0017
   1-T25        |time to go :        14.00    |                                  1-T19
    -1          |_____________________________|                                   -1
                 ______________B|______________
                | 1-T13  -1                   |
                |x100 ripple in               |
                |                             |
                |                             |
                |weighting  :+0.00000000      | G
                |                             |----------------------------------------
                |time so far:         6.00    |                                 to page
                |cost to go :         5.00    |                                  0016
                |time to go :         5.00    |                                  1-T10
                |_____________________________|                                   -1
                 ______________B|______________      ____________________________
                | 1-T14  -1                   |     |  ****** FAULT ******       |
                |x 10 ripple in               |     |                            |
                |                             |     |Sus AG Ref#:    11          |
                |                             |     |                            |
                |weighting  :+0.00000000      | G   |cumulative totals           |
                |                             |-----|      tests:     5          |
                |time so far:         7.00    |     | test cost:          8.00   |
                |cost to go :         4.00    |     | test time:          8.00   |
                |time to go :         4.00    |     | enclosures:     1          |
                |_____________________________|     |____________________________|
                 ______________B|______________      ____________________________
                | 1-T15  -1                   |     |  ****** FAULT ******       |
                |x1 counter out               |     |                            |
                |                             |     |Sus AG Ref#:    10          |
                |                             |     |                            |
                |weighting  :+0.00000000      | G   |cumulative totals           |
                |                             |-----|      tests:     6          |
                |time so far:         8.00    |     | test cost:          9.00   |
                |cost to go :         3.00    |     | test time:          9.00   |
                |time to go :         3.00    |     | enclosures:     1          |
                |_____________________________|     |____________________________|
                              B|   FAULT
              to page 0015     |   9
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
                    from page |   1-T15
                      0014    |    -1
                  ___________B|___________
                 |  ****** FAULT ******   |
                 |                        |
                 |Sus AG Ref#:     9      |
                 |                        |
                 |cumulative totals       |
                 |      tests:     6      |
                 |  test cost:       9.00 |
                 |  test time:       9.00 |
                 | enclosures:     1      |
                 |________________________|


                  ________________________      ________________________
                 |  1-T10  -1             |    |  ****** FAULT ******   |
                 |x100 counter out        |    |                        |
                 |                        |    |Sus AG Ref#:    13      |
                 |                        |    |                        |
       G         |weighting  :+0.00000000 | G  |cumulative totals       |
    ----------|                        |---|      tests:     5      |
    from page    |time so far:       7.00 |    |  test cost:       8.00 |
      0014       |cost to go :       4.00 |    |  test time:       8.00 |
      1-T13      |time to go :       3.00 |    | enclosures:     1      |
       -1        |________________________|    |________________________|
                  ___________B|___________
                 |  ****** FAULT ******   |
                 |                        |
                 |Sus AG Ref#:    12      |
                 |                        |
                 |cumulative totals       |
                 |      tests:     5      |
                 |  test cost:       8.00 |
                 |  test time:       8.00 |
                 | enclosures:     1      |
                 |________________________|
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
             ________________________
            |  1-T19  -1             |
            |VFAKE inverse           |
            |                        |
            |                        |
    G       |weighting  :+0.00000000 | G
------------|                        |---------------------------------------
from page   |time so far:       6.00 |                                  to page
  0014      |cost to go :      11.00 |                                   0018
  1-T16     |time to go :      10.00 |                                   1-T20
    -1      |________________________|                                     -1
             ___________B|___________     ________________________
            |  1-T18  -1             |   |  ****** FAULT ******   |
            |count 9 HSYNC pulse     |   |                        |
            |                        |   |Sus AG Ref#:    16      |
            |                        |   |                        |
            |weighting  :+0.00000000 | G |cumulative totals       |
            |                        |---|      tests:     5      |
            |time so far:       7.00 |   | test cost:        9.00 |
            |cost to go :      10.00 |   | test time:        9.00 |
            |time to go :       9.00 |   | enclosures:     1      |
            |________________________|   |________________________|
             ___________B|___________     ________________________
            |  1-T17  -1             |   |  ****** FAULT ******   |
            |count 262 pulse         |   |                        |
            |                        |   |Sus AG Ref#:    15      |
            |                        |   |                        |
            |weighting  :+0.00000000 | G |cumulative totals       |
            |                        |---|      tests:     6      |
            |time so far:       9.00 |   | test cost:       13.00 |
            |cost to go :       8.00 |   | test time:       13.00 |
            |time to go :       7.00 |   | enclosures:     1      |
            |________________________|   |________________________|
             ___________B|___________
            |  ****** FAULT ******   |
            |                        |
            |Sus AG Ref#:    14      |
            |                        |
            |cumulative totals       |
            |      tests:     6      |
            | test cost:       13.00 |
            | test time:       13.00 |
            | enclosures:     1      |
            |________________________|
```

FAULT ISOLATION INDICATOR REPORT

DETAIL ANALYSIS

Diagnostic Flow Diagram

```
            ________________________       ________________________
           | 1-T20  -1              |     |  ****** FAULT ******   |
           |VFAKE & non-intrl       |     |                        |
           |                        |     |Sus AG Ref#:   18       |
           |                        |     |                        |
    G      |weighting  :+0.00000000 |  G  |cumulative totals       |
 ----------|                        |-----|      tests:     5      |
 from page |time so far:       7.00 |     |  test cost:       8.00 |
   0017    |cost to go :       2.00 |     |  test time:       8.00 |
   1-T19   |time to go :       3.00 |     | enclosures:     1      |
    -1     |________________________|     |________________________|
            ___________B|___________
           |  ****** FAULT ******   |
           |                        |
           |Sus AG Ref#:   17       |
           |                        |
           |cumulative totals       |
           |      tests:     5      |
           |  test cost:       8.00 |
           |  test time:       8.00 |
           | enclosures:     1      |
           |________________________|


            ________________________       ________________________
           | 1-T27  -1              |     |                        |
           |HNEW inverse out        |     |  NO FAULTS ENCOUNTERED |
           |                        |     |                        |
           |                        |     |                        |
    G      |weighting  :+0.00000000 |  G  |cumulative totals       |
 ----------|                        |-----|      tests:     2      |
 from page |time so far:       1.00 |     |  test cost:       2.00 |
   0009    |cost to go :       2.00 |     |  test time:       2.00 |
   1-T26   |time to go :       3.00 |     | enclosures:     1      |
    -1     |________________________|     |________________________|
            ___________B|___________
           |  ****** FAULT ******   |
           |                        |
           |Sus AG Ref#:   19       |
           |                        |
           |cumulative totals       |
           |      tests:     2      |
           |  test cost:       2.00 |
           |  test time:       2.00 |
           | enclosures:     1      |
           |________________________|
```

APPENDIX 3

EXAMPLE DATA ENCODING FORMAT

STAT-PAWS DATA ENCODING FORMAT

Partial description of STAT - PAWS interchange format

Description of Field	Format of Field	Example
Start Model Definition System & Model numbers	$@Start_Mdl_Definition@$ S-###M-####	$@Start_Mdl_Definition@$ S-1M-10
Model Description Header Model Description	$?Mdl_Description?$ XXXXXXXXXXXXXXXXXXXXXXXXX (up to 25 characters)	$?Mdl_Description?$ Example Model
Model Comment Header Comment Line 1 Comment Line 2 . . . Comment Line 25	$?Mdl_Comment?$ XXXXXXXXXXXXXXXX... XXXXXXXXXXXXXXXX... . . . XXXXXXXXXXXXXXXX... (each line is of variable length - Total Comment may be up to 1000 characters)	$?Mdl_Comment?$ This is a Model Comment for Model 10 . . . This is the last line.
Test User Char. Name Header Test User Char. Name	$?Test_User_Char_Name?$ XXXXXXXXXXXXXXX (up to 15 characters)	$?Test_User_Char_Name?$ Criticality
Item User Char. Name Header Item User Char. Name	$?Item_User_Char_Name?$ XXXXXXXXXXXXXXX (up to 15 characters)	$?Item_User_Char_Name?$ Availability

TABLE C-1 (Standard Import/Export File Format Definitions)

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Description of Field	Format of Field	Example
Item Definition Header Item Root number	$@Define_Item@$ I####	$@Define_Item@$ I100
Item Description Header Item Description	$?Item_Description?$ XXXXXXXXXXXXXXXXXXXXXXXXX (up to 19 characters)	$?Item_Description?$ X5230
Item Cost Header Cost to Replace Item	$?Item_Cost?$ #######.## mandatory decimal point Range: 0.00 to 9999999.99	$?Item_Cost?$ 30.50
Item Time Header Time to Replace Item	$?Item_Time?$ #######.## mandatory decimal point Range: 0.00 to 9999999.99	$?Item_Time?$ 30.50
Item Failure Rate Header Item Failure Rate	$?Item_Failure_Rate?$ #######.## mandatory decimal point Range: 0.00 to 9999999.99	$?Item_Failure_Rate?$ 0.00010882

TABLE C-1 (Standard Import/Export File Format Definitions - continued)

116

Description of Field	Format of Field	Example
Item User Char. Header Item User Characteristic	$?Item_User_Char?$ #######.## mandatory decimal point Range: 0.00000001 to 9999999.99	$?Item_User_Char?$ 100.53
Item Aspect Definition Header Item Aspect Number	$@Define_Item_Aspect@$ ####	$@Define_Item_Aspect@$ 1
Item Aspect Description Header Item Aspect Description	$?I_Asp_Description?$ XXXXXXXXXXXXXXXXXXXXXXXXX (up to 19 characters)	$?I_Asp_Description?$ X5230 Pin 12
Detectability Header Item Aspect Detectability D = Detectable N = Non-Detectable	$?Detectability?$ X	$?Detectability?$ D
FR Apportionment Header Failure Rate Apportionment	$?Apportionment?$ ###	$?Apportionment?$ 1

TABLE C-1 (Standard Import/Export File Format Definitions - continued)

117

Description of Field	Format of Field	Example
Test Definition Header Test Root and Aspect numbers	$@Define_Test@$ T####-####	$@Define_Test@$ T100-1
Test Category Header Test Category D = Defined Test U = Undefined Test E = Equate Test	$?Test_Category?$ X	$?Test_Category?$ D
Test Description Header Test Description	$?Test_Description?$ XXXXXXXXXXXXXXXXXXXXXXXXX (up to 19 characters)	$?Test_Description?$ Test Input to X
Test Type Header Test Type P = Probe E = External B = BIT/BITE	$?Test_Type?$ X	$?Test_Type?$ P
Test Cost Header Test Cost	$?Test_Cost?$ #######.## mandatory decimal point Range: 0.00 to 9999999.99	$?Test_Cost?$ 30.50

TABLE C-1 (Standard Import/Export File Format Definitions - continued)

811

Description of Field	Format of Field	Example
Test Time Header Test Time	$?Test_Time?$ #######.## mandatory decimal point Range: 0.00 to 9999999.99	$?Test_Time?$ 30.50
Test User Char. Header Test User Characteristic	$?Test_User_Char?$ #######.## mandatory decimal point Range: 0.00000001 to 9999999.99	$?Test_User_Char?$ 30.50
Test Enclosure Header Enclosure Number	$?Test_Enclosure?$ ### Range: 1 to 999	$?Test_Enclosure?$ 1
Test Level Header Level Number	$?Test_Level?$ ### Range 1 to 9	$?Test_Level?$ 2

TABLE C-1 (Standard Import/Export File Format Definitions - continued)

Description of Field	Format of Field	Example
Dependencies Header	$@Dependencies@$	$@Dependencies@$
Item Aspect Dependency 1	I####-####	I15-7
Cause Test 1	T####-####	T1001-1
Cause Test 2	T####-####	T1002-1
Item Aspect Dependency 2	I####-####	I15-8
Cause Test 3	T####-####	T15-3
.	.	.
.	.	.
.	.	.
Item Aspect Dependency N	I####-####	I231-1
Cause Test X	T####-####	T9250-112
Note: Each Cause Test is listed IMMEDIATELY following the Item Aspect Dependency to which it relates. Each Dependency may appear only once. Equate Tests have only Cause Test Dependencies. Normal Tests either have both Item Aspect Dependencies and Cause Tests, or (as in the case of an Input Test) no dependencies at all.		
End Model Definition	$@End_Mdl_Definition@$	$@End_Mdl_Definition@$

TABLE C-1 (Standard Import/Export File Format Definitions - continued)

119

```
$@Start_Mdl_Definition@$
S-1M-10
$?Mdl_Description?$
Sample Diagram
$?Mdl_Comment?$
This example Model has been
designed to demonstrate the
Import/Export File Format.
$?Test_User_Char_Name?$
Criticality
$?Item_User_Char_Name?$
Availability
$@Define_Item@$
I1
$?Item_Description?$
Block A
$?Item_Cost?$
12.75
$?Item_Time?$
20.00
$?Item_Failure_Rate?$
0.00010620
$?Item_User_Char?$
100.53
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block A - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I2
?Item_Description?$
Block B
$?Item_Cost?$
102.50
$?Item_Time?$
110.00
$?Item_Failure_Rate?$
0.00001250
$?Item_User_Char?$   52.50
$@Define_Item_Aspect@$
1
```

FIGURE C-2 (Sample Import/Export File)

130

```
$?_I_Asp_Description?$
Block B - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I3
$?Item_Description?$
Block C
$?Item_Cost?$
180.00
$?Item_Time?$
150.00
$?Item_Failure_Rate?$
0.00000528
$?Item_User_Char?$
2.00
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block C - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I4
$?Item_Description?$
Block D
$?Item_Cost?$
5.00
$?Item_Time?$
10.00
$?Item_Failure_Rate?$
0.00012500
$?Item_User_Char?$
98.60
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block D - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$@Define_Item_Aspect@$
2
$?_I_Asp_Description?$
Block D - Pin 2
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I5
$?Item_Description?$
Block E
$?Item_Cost?$
400.00
$?Item_Time?$
20.00
$?Item_Failure_Rate?$
0.00009520
$?Item_User_Char?$
100.53
$@Define_Item_Aspect@$
  1
$?_I_Asp_Description?$
Block E - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I6
$?Item_Description?$
Block F
$?Item_Cost?$
12.75
$?Item_Time?$
20.00
$?Item_Failure_Rate?$
0.00010620
$?Item_User_Char?$
100.53
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block F - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$@Define_Item@$
I7
$?Item_Description?$
Block G
$?Item_Cost?$
89.99
$?Item_Time?$
35.50
$?Item_Failure_Rate?$
0.00007800
$?Item_User_Char?$
100.53
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block G - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Item@$
I8
$?Item_Description?$
Block H
$?Item_Cost?$
20.50
$?Item_Time?$
19.44
$?Item_Failure_Rate?$
0.00026667
$?Item_User_Char?$
10.00
$@Define_Item_Aspect@$
1
$?_I_Asp_Description?$
Block H - Pin 1
$?Detectability?$
D
$?Apportionment?$
1
$@Define_Test@$
T1-1
$?Test_Category?$
D
$?Test_Description?$
Input to Block A
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$?Test_Type?$
P
$?Test_Cost?$
35.00
$?Test_Time?$
7.00
$?Test_User_Char?$
500.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
$@Define_Test@$
T2-1
$?Test_Category?$
D
$?Test_Description?$
Input to Block D
$?Test_Type?$
P
$?Test_Cost?$
107.00
$?Test_Time?$
23.50
$?Test_User_Char?$
150.75
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
$@Define_Test@$
T3-1
$?Test_Category?$
D
$?Test_Description?$
Input to Block G
$?Test_Type?$
P
$?Test_Cost?$
103.00
$?Test_Time?$
1005.00
$?Test_User_Char?$
10.00
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
$@Define_Test@$
T4-1
$?Test_Category?$
D
$?Test_Description?$
Test @ I1-1
$?Test_Type?$
P
$?Test_Cost?$
195.00
$?Test_Time?$
32.50
$?Test_User_Char?$
500.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I1-1
T1-1
$@Define_Test@$
T5-1
$?Test_Category?$
D
$?Test_Description?$
Output @ I3-1
$?Test_Type?$
P
$?Test_Cost?$
240.00
$?Test_Time?$
5.00
$?Test_User_Char?$
100.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I3-1
I2-1
T4-1
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$@Define_Test@$
T6-1
$?Test_Category?$
D
$?Test_Description?$
Output @ I4-1
$?Test_Type?$
P
$?Test_Cost?$
35.00
$?Test_Time?$
7.00
$?Test_User_Char?$
500.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I4-1
T4-1
T11-1
$@Define_Test@$
T7-1
$?Test_Category?$
D
$?Test_Description?$
Output @ I6-1
$?Test_Type?$
P
$?Test_Cost?$
45.00
$?Test_Time?$
5.00
$?Test_User_Char?$
40.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I6-1
T10-1
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$@Define_Test@$
T8-1
$?Test_Category?$
D
$?Test_Description?$
Output @ I8-1
$?Test_Type?$
P
$?Test_Cost?$
100.00
$?Test_Time?$
100.00
$?Test_User_Char?$
5.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I8-1
T9-1
$@Define_Test@$
T9-1
$?Test_Category?$
D
$?Test_Description?$
Test @ I7-1
$?Test_Type?$
P
$?Test_Cost?$
35.00
$?Test_Time?$
7.00
$?Test_User_Char?$
500.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I7-1
T3-1
```

FIGURE C-2 (Sample Import/Export File - continued)

```
$@Define_Test@$
T10-1
$?Test_Category?$
D
$?Test_Description?$
Test @ I4-2
$?Test_Type?$
P
$?Test_Cost?$
125.75
$?Test_Time?$
130.00
$?Test_User_Char?$
25.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I4-2
T2-1
T11-1
$@Define_Test@$
T11-1
$?Test_Category?$
D
$?Test_Description?$
Test @ I5-1
$?Test_Type?$
P
$?Test_Cost?$
35.00
$?Test_Time?$
21.00
$?Test_User_Char?$
65.00
$?Test_Enclosure?$
1
$?Test_Level?$
1
$@Dependencies@$
I5-1
T3-1
$@End_Mdl_Definition@$
```

FIGURE C-2 (Sample Import/Export File - continued)

APPENDIX 4

Dependency Model for the High Voltage Power Supply from the AV-8B Heads-up Display, HV-A2.

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Weight Printed is Time of making test

Test	1	Label = TA2P1-1	Weight = 3.00
Test	2	Label = TA2P1-11	Weight = 3.00
Test	3	Label = TA2P1-12	Weight = 3.00
Test	4	Label = TA2P1-13	Weight = 3.00
Test	5	Label = TA2P1-14	Weight = 3.00
Test	6	Label = TA2P1-17	Weight = 3.00
Test	7	Label = TA2P1-19	Weight = 3.00
Test	8	Label = TA2P1-2	Weight = 3.00
Test	9	Label = TA2P1-20	Weight = 3.00
Test	10	Label = TA2P1-23	Weight = 3.00
Test	11	Label = TA2P1-24	Weight = 3.00
Test	12	Label = TA2P1-25	Weight = 3.00
Test	13	Label = TA2P1-26	Weight = 3.00
Test	14	Label = TA2P1-27	Weight = 3.00
Test	15	Label = TA2P1-29	Weight = 3.00
Test	16	Label = TA2P1-3	Weight = 3.00
Test	17	Label = TA2P1-30	Weight = 3.00
Test	18	Label = TA2P1-31	Weight = 3.00
Test	19	Label = TA2P1-32	Weight = 3.00
Test	20	Label = TA2P1-33	Weight = 3.00
Test	21	Label = TA2P1-34	Weight = 3.00
Test	22	Label = TA2P1-36	Weight = 3.00
Test	23	Label = TA2P1-37	Weight = 3.00
Test	24	Label = TA2P1-5	Weight = 3.00
Test	25	Label = TA2P1-6	Weight = 3.00
Test	26	Label = TA2P1-7	Weight = 3.00
Test	27	Label = TA2P1-8	Weight = 3.00
Test	28	Label = TA2P1-9	Weight = 3.00
Test	29	Label = TP1-A2	Weight = 3.00
Test	30	Label = TP2-A2	Weight = 3.00
Test	31	Label = TP3-A2	Weight = 3.00
Test	32	Label = TP4-A2	Weight = 3.00
Test	33	Label = TXA2P1-11	Weight = 3.00
Test	34	Label = TXA2P1-13	Weight = 3.00
Test	35	Label = TXA2P1-23	Weight = 3.00
Test	36	Label = TXA2P1-14	Weight = 3.00
Test	37	Label = TXA2P1-7	Weight = 3.00
Test	38	Label = TYA2P1-20	Weight = 3.00
Test	39	Label = TXA2P1-8	Weight = 3.00
Test	40	Label = TXP3-A2	Weight = 3.00
Test	41	Label = TXP4-A2	Weight = 3.00
Test	42		

		Label =	TYA2P1-17	Weight =	3.00
Test	43	Label =	TR16	Weight =	3.00
Test	45	Label =	TR17	Weight =	3.00
Test	47	Label =	TR33	Weight =	3.00
Test	48	Label =	TR35	Weight =	3.00
Test	49	Label =	TPA-A2	Weight =	3.00
Test	50	Label =	TXA2P1-25	Weight =	3.00
Test	51	Label =	TXA2P1-32	Weight =	3.00
Test	52	Label =	T+30STTO	Weight =	3.00
Test	53	Label =	T+15STTO	Weight =	3.00
Test	5[illegible]	Label =	T-15STTO	Weight =	3.00
Test	55	Label =	TR14	Weight =	3.00
Test	56	Label =	TYA2P1-8	Weight =	3.00

End of weight display. Weight= Time of making test

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Test 1 Label = (TE1) TA2P1-1
Conditionals:

Test 2 Label = (TE2) TA2P1-11
Conditionals:

Test 3 Label = (TE3) TA2P1-12
Conditionals:

Test 4 Label = (TE4) TA2P1-13
Conditionals:

Test 5 Label = (TE5) TA2P1-14
Conditionals:

Test 6 Label = (TE6) TA2P1-17
Conditionals:

Test 7 Label = (TE7) TA2P1-19
Conditionals:

Test 8 Label = (TE8) TA2P1-2
Conditionals:

Test 9 Label = (TE9) TA2P1-20
Conditionals:

Test 10 Label = (TE10) TA2P1-23
Conditionals:

Test 11 Label = (TE11) TA2P1-24
Conditionals:

Test 12 Label = (TE12) TA2P1-25
Conditionals:

Test 13 Label = (TE13) TA2P1-26
Conditionals:

Test 14 Label = (TE14) TA2P1-27
Conditionals:

Test 15 Label = (TE15) TA2P1-29
Conditionals:

Test 16 Label = (TE16) TA2P1-3
Conditionals:

Test 17 Label = (TE17) TA2P1-30
Conditionals:

Test 18 Label = (TE18) TA2P1-31
Conditionals:

Test 19 Label = (TE19) TA2P1-32

```
Conditionals:

Test    20    Label = (TE20)    TA2P1-33
Conditionals:

Test    21    Label = (TE21)    TA2P1-34
Conditionals:

Test    22    L
```

abel = (TE22) TA2P1-36
Conditionals:

Test 23 Label = (TE23) TA2P1-37
Conditionals:

Test 24 Label = (TE24) TA2P1-5
Conditionals:

Test 25 Label = (TE25) TA2P1-6
Conditionals:

Test 26 Label = (TE26) TA2P1-7
Conditionals:

Test 27 Label = (TE27) TA2P1-8
Conditionals:

Test 28 Label = (TE28) TA2P1-9
Conditionals:

Test 29 Label = (TE29) TP1-A2
Conditionals:

Test 30 Label = (TE30) TP2-A2
Conditionals:

Test 31 Label = (TE31) TP3-A2
Conditionals:

Test 32 Label = (TE32) TP4-A2
Conditionals:

Test 33 Label = (TE33) TXA2P1-11
Conditionals:

Test 34 Label = (TE34) TXA2P1-13
Conditionals:

Test 35 Label = (TE35) TXA2P1-23
Conditionals:

Test 36 Label = (TE36) TXA2P1-14
Conditionals:

Test 37 Label = (TE37) TXA2P1-7
Conditionals:

Test 38 Label = (TE38) TYA2P1-20
Conditionals:

Test 39 Label = (TE39) TXA2P1-8
Conditionals:

Test 40 Label = (TE40) TXP3-A2
Conditionals:

Test 41 Label = (TE41) TXP4-A2
Conditionals:

```
Test   42   Label = (TE42)   TYA2P1-17
Conditionals:

Test   43   Label = (TE43)   TR16
Conditionals:

Test   45   Label = (TE45)   TR17
Conditionals:

Test   47   Label = (TE47)   TR33
Conditionals:

Test   48   Label = (TE48)   TR35
Conditionals:

Test   49   Label = (TE49)   TPA-A2
Conditionals:

Test   50   Label = (TE50)   TXA2P1-25
Conditionals:

Test   51   Label = (TE51)   TXA2P1-32
Conditionals:

Test   52   Label = (TE52)   T+30STTO
Conditionals:

Test   53   Label = (TE53)   T+15STTO
Conditionals:

Test   54   Label = (TE54)   T-15STTO
Conditionals:

Test   55   Label = (TE55)   TR14
Conditionals:

Test   56   Label = (TE56)   TYA2P1-8
Conditionals:

End of conditional display
```

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Weight Printed is Failure Frequencies

Component	1	Label =	A2C1	Weight =	0.00600
Component	3	Label =	A2C11	Weight =	0.00600
Component	5	Label =	A2C2	Weight =	0.00600
Component	6	Label =	A2C3	Weight =	0.00600
Component	7	Label =	A2C6	Weight =	0.00600
Component	8	Label =	A2C7	Weight =	0.00600
Component	9	Label =	A2C8	Weight =	0.00600
Component	11	Label =	A2CR1	Weight =	0.01500
Component	12	Label =	A2CR10	Weight =	0.01500
Component	13	Label =	A2CR11	Weight =	0.01500
Component	14	Label =	A2CR12	Weight =	0.01500
Component	15	Label =	A2CR2	Weight =	0.01500
Component	16	Label =	A2CR3	Weight =	0.01500
Component	17	Label =	A2CR4	Weight =	0.01500
Component	18	Label =	A2CR5	Weight =	0.01500
Component	19	Label =	A2CR6	Weight =	0.01500
Component	20	Label =	A2CR7	Weight =	0.01500
Component	21	Label =	A2CR8	Weight =	0.01500
Component	22	Label =	A2CR9	Weight =	0.01500
Component	23	Label =	A2Q1	Weight =	2.80000
Component	24	Label =	A2Q2	Weight =	2.80000
Component	25	Label =	A2Q3	Weight =	0.05800
Component	26	Label =	A2Q4	Weight =	0.05800
Component	27	Label =	A2		

		Q5	Weight = 0.05800
Component	28	Label = A2Q6	Weight = 0.05800
Component	29	Label = A2Q7	Weight = 0.05800
Component	30	Label = A2Q8	Weight = 0.09400
Component	31	Label = A2R1	Weight = 0.00360
Component	32	Label = A2R10	Weight = 0.00360
Component	33	Label = A2R11	Weight = 0.00360
Component	34	Label = A2R12	Weight = 0.00360
Component	35	Label = A2R13	Weight = 0.00360
Component	40	Label = A2R18	Weight = 0.00360
Component	41	Label = A2R19	Weight = 0.00360
Component	42	Label = A2R2	Weight = 0.00360
Component	43	Label = A2R20	Weight = 0.00360
Component	44	Label = A2R21	Weight = 0.00360
Component	45	Label = A2R22	Weight = 0.00360
Component	46	Label = A2R23	Weight = 0.00360
Component	47	Label = A2R24	Weight = 0.00360
Component	48	Label = A2R25	Weight = 0.00360
Component	49	Label = A2R26	Weight = 0.00360
Component	50	Label = A2R27	Weight = 0.00360
Component	51	Label = A2R28	Weight = 0.00360
Component	52	Label = A2R29	Weight = 0.00360
Component	53	Label = A2R3	Weight = 0.00360
Component	54	Label = A2R30	Weight = 0.00360
Component	55	Label = A2R31	Weight = 0.00360
Component	56	Label = A2R32	Weight = 0.00360
Component	57	Label = A2R33	Weight = 0.00360
Component	58	Label = A2R34	Weight = 0.00360
Component	60	Label = A2R4	Weight = 0.00360
Component	61	Label = A2R5	Weight = 0.00360
Component	62	Label = A2R6	Weight = 0.00360
Component	63	Label = A2R7	Weight = 0.00360
Component	64	Label = A2R8	Weight = 0.00360
Component	65	Label = A2R9	Weight = 0.00360
Component	66	Label = A2U1A	Weight = 0.05000
Component	67	Label = A2VR1	Weight = 0.06200
Component	68	Label = GNDA	Weight = 0.00000
Component	69	Label = GNDC	Weight = 0.00000
Component	70	Label = GNDD	Weight = 0.00000
Component	71	Label = A2C7S	Weight = 0.00600
Component	72	Label = A2C6S	Weight = 0.00600
Component	73	Label = A2CR8S	Weight = 0.01500
Component	74	Label = A2CR7S	Weight = 0.01500
Component	77	Label = A2Q3OE	Weight = 0.05800
Component	78	Label = A2CR6S	Weight = 0.01500
Component	79	Label = A2Q2OE	Weight = 0.05800
Component	80	Label = A2Q5OE	Weight = 0.05800
Component	81	Label = A2C9	Weight = 0.00600
Component	82	Label = A2C10	Weight = 0.00600
Component	84	Label = A2R15	Weight = 0.00360
Component	86	Label = A2U1-3	Weight = 0.05000
Component	91	Label = A2VR1S	Weight = 0.01500
Component	92	Label = A2R35	Weight = 0.00360
Component	93	Label = A2C12	Weight = 0.00600
Component	94	Label = A2R17	Weight = 0.00360
Component	95	Label = A2R14	Weight = 0.00360
Component	96	Label = A2R16	Weight = 0.00360
Component	98	Label = A2U1-11	Weight = 0.05000
Component	100	Label = A2U1-4	Weight = 0.00000
Component	101	Label = A2C8S	Weight = 0.00000

Component 102	Label = A2U1-2	Weight =	0.00000
Component 103	Label = A2C2S	Weight =	0.00600
Component 105	Label = A2CR12S	Weight =	0.01500
Component 106	Label = A2VR1M	Weight =	0.01500
RTOK (Retest OK)		Weight =	0.05000

End of weight display. Weight= Failure Frequencies

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Associated test group TINPUT

(TE1)	TA2P1-1	(TE2)	TA2P1-11	(TE4)	TA2P1-13
(TE5)	TA2P1-14	(TE7)	TA2P1-19	(TE8)	TA2P1-2
(TE9)	TA2P1-20	(TE10)	TA2P1-23	(TE14)	TA2P1-27
(TE16)	TA2P1-3	(TE18)	TA2P1-31	(TE23)	TA2P1-37
(TE26)	TA2P1-7				

Associated test group TXINPUT

(TE33)	TXA2P1-11	(TE34)	TXA2P1-13	(TE35)	TXA2P1-23
(TE36)	TXA2P1-14	(TE37)	TXA2P1-7	(TE38)	TYA2P1-20

Associated test group TNOACCESS

(TE3)	TA2P1-12	(TE6)	TA2P1-17	(TE12)	TA2P1-25
(TE17)	TA2P1-30	(TE19)	TA2P1-32	(TE22)	TA2P1-36
(TE27)	TA2P1-8	(TE30)	TP2-A2	(TE31)	TP3-A2
(TE32)	TP4-A2	(TE49)	TPA-A2	(TE51)	TXA2P1-32

Associated test group TDFC

(TE42)	TYA2P1-17	(TE56)	TYA2P1-8

Associated test group TSTTO

(TE52)	T+30STTO	(TE53)	T+15STTO	(TE54)	T-15STTO

Associated test group TOSC

(TE13)	TA2P1-26	(TE21)	TA2P1-34	(TE24)	TA2P1-5
(TE28)	TA2P1-9				

End of associated test group display

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Test 1 Label = (TE1) TA2P1-1
Dependencies:

Test 2 Label = (TE2) TA2P1-11
Dependencies:

Test 3 Label = (TE3) TA2P1-12
Dependencies:
(TE28) TA2P1-9

Test 4 Label = (TE4) TA2P1-13
Dependencies:

Test 5 Label = (TE5) TA2P1-14
Dependencies:

(TE2)	TA2P1-11	(CP70)	GNDD

Test 6 Label = (TE6) TA2P1-17
Dependencies:

(TE4)	TA2P1-13	(TE5)	TA2P1-14	(TE9)	TA2P1-20
(TE10)	TA2P1-23	(TE26)	TA2P1-7	(TE30)	TP2-A2
(CP9)	A2C8	(CP12)	A2CR10	(CP13)	A2CR11
(CP14)	A2CR12	(CP22)	A2CR9	(CP28)	A2Q6
(CP29)	A2Q7	(CP30)	A2Q8	(CP40)	A2R18
(CP41)	A2R19	(CP43)	A2R20	(CP44)	A2R21
(CP46)	A2R23	(CP47)	A2R24	(CP49)	A2R26
(CP50)	A2R27	(CP51)	A2R28	(CP52)	A2R29

(CP54) A2R30 (CP56) A2R32 (CP66) A2U1A
(CP68) GNDA

Test 7 Label = (TE7) TA2P1-19
Dependencies:

Test 8 Label = (TE8) TA2P1-2
Dependencies:

Test 9 Label = (TE9) TA2P1-20
Dependencies:

Test 10 Label = (TE10) TA2P1-23
Dependencies:

Test 11 Label = (TE11) TA2P1-24
Dependencies:
(TE10) TA2P1-23 (TE14) TA2P1-27 (TE23) TA2P1-37
(CP19) A2CR6 (CP25) A2Q3 (CP63) A2R7
(CP64) A2R8 (CP67) A2VR1 (CP68) GNDA
(CP106) A2VR1M

Test 12 Label = (TE12) TA2P1-25
Dependencies:
(TE10) TA2P1-23 (CP7) A2C6 (CP8) A2C7
(CP21) A2CR8 (CP68) GNDA

Test 13 Label = (TE13) TA2P1-26
Dependencies:
(TE7) TA2P1-19 (TE10) TA2P1-23 (TE18) TA2P1-31
(CP27) A2Q5 (CP32) A2R10 (CP33) A2R11
(CP34) A2R12 (CP35) A2R13 (CP68) GNDA
(CP80) A2Q5OE

Test 14 Label = (TE14) TA2P1-27
Dependencies:

Test 15 Label = (TE15) TA2P1-29
Dependencies:
(TE10) TA2P1-23 (TE12) TA2P1-25 (TE19) TA2P1-32
(CP7) A2C6 (CP8) A2C7 (CP20) A2CR7
(CP21) A2CR8 (CP68) GNDA (CP71) A2C7S
(CP72) A2C6S (CP73) A2CR8S (CP74) A2CR7S

Test 16 Label = (TE16) TA2P1-3
Dependencies:

Test 17 Label = (TE17) TA2P1-30
Dependencies:
(TE10) TA2P1-23 (TE11) TA2P1-24 (TE14) TA2P1-27
(TE23) TA2P1-37 (CP6) A2C3 (CP19) A2CR6
(CP25) A2Q3 (CP64) A2R8 (CP67) A2VR1
(CP68) GNDA (CP77) A2Q3OE (CP78) A2CR6S
(CP91) A2VR1S

Test 18 Label = (TE18) TA2P1-31
Dependencies:

Test 19 Label = (TE19) TA2P1-32

Dependencies:

(TE10)	TA2P1-23	(CP7)	A2C6	(CP8)	A2C7
(CP21)	A2CR8	(CP68)	GNDA		

Test 20 Label = (TE20) TA2P1-33
Dependencies:

(TE10)	TA2P1-23	(TE14)	TA2P1-27	(TE23)	TA2P1-37
(CP19)	A2CR6	(CP64)	A2R8	(CP67)	A2VR1
(CP68)	GNDA	(CP77)	A2Q3OE	(CP78)	A2CR6S

Test 21 Label = (TE21) TA2P1-34
Dependencies:

(TE22)	TA2P1-36	(CP65)	A2R9

Test 22 Label = (TE22) TA2P1-36
Dependencies:

(TE7)	TA2P1-19	(TE10)	TA2P1-23	(TE18)	TA2P1-31
(CP26)	A2Q4	(CP32)	A2R10	(CP33)	A2R11
(CP34)	A2R12	(CP35)	A2R13	(CP68)	GNDA
(CP80)	A2Q5OE				

Test 23 Label = (TE23) TA2P1-37
Dependencies:

Test 24 Label = (TE24) TA2P1-5
Dependencies:

(TE1)	TA2P1-1	(TE8)	TA2P1-2	(TE16)	TA2P1-3
(CP5)	A2C2	(CP17)	A2CR4	(CP24)	A2Q2
(CP60)	A2R4	(CP61)	A2R5	(CP69)	GNDC
(CP79)	A2Q2OE	(CP103)	A2C2S		

Test 25 Label = (TE25) TA2P1-6
Dependencies:

(TE1)	TA2P1-1	(CP18)	A2CR5	(CP69)	GNDC

Test 26 Label = (TE26) TA2P1-7
Dependencies:

Test 27 Label = (TE27) TA2P1-8
Dependencies:

(TE4)	TA2P1-13	(TE5)	TA2P1-14	(TE10)	TA2P1-23
(TE26)	TA2P1-7	(TE30)	TP2-A2	(CP9)	A2C8
(CP40)	A2R18	(CP41)	A2R19	(CP43)	A2R20
(CP44)	A2R21	(CP45)	A2R22	(CP66)	A2U1A
(CP68)	GNDA				

Test 28 Label = (TE28) TA2P1-9
Dependencies:

(TE1)	TA2P1-1	(TE8)	TA2P1-2	(TE16)	TA2P1-3
(CP1)	A2C1	(CP11)	A2CR1	(CP15)	A2CR2
(CP16)	A2CR3	(CP23)	A2Q1	(CP42)	A2R2
(CP53)	A2R3	(CP61)	A2R5	(CP69)	GNDC
(CP79)	A2Q2OE	(CP103)	A2C2S		

Test 29 Label = (TE29) TP1-A2
Dependencies:

(TE10)	TA2P1-23	(TE11)	TA2P1-24	(TE14)	TA2P1-27
(TE23)	TA2P1-37	(CP6)	A2C3	(CP19)	A2CR6
(CP25)	A2Q3	(CP62)	A2R6	(CP64)	A2R8
(CP67)	A2VR1	(CP68)	GNDA	(CP77)	A2Q3OE

(CP78)	A2CR6S	(CP91)	A2VR1S	(CP106)	A2VR1M

Test 30 Label = (TE30) TP2-A2
Dependencies:

(TE2)	TA2P1-11	(TE4)	TA2P1-13	(TE5)	TA2P1-14
(TE7)	TA2P1-19	(TE9)	TA2P1-20	(TE10)	TA2P1-23
(TE26)	TA2P1-7	(TE30)	TP2-A2	(CP3)	A2C11
(CP9)	A2C8	(CP12)	A2CR10	(CP22)	A2CR9
(CP28)	A2Q6	(CP29)	A2Q7	(CP30)	A2Q8
(CP40)	A2R18	(CP41)	A2R19	(CP43)	A2R20
(CP44)	A2R21	(CP46)	A2R23	(CP47)	A2R24
(CP49)	A2R26	(CP50)	A2R27	(CP51)	A2R28

(CP52)	A2R29	(CP54)	A2R30	(CP57)	A2R33
(CP58)	A2R34	(CP66)	A2U1A	(CP68)	GNDA
(CP70)	GNDD				

Test 31 Label = (TE31) TP3-A2
Dependencies:

(TE9)	TA2P1-20	(CP48)	A2R25	(CP49)	A2R26

Test 32 Label = (TE32) TP4-A2
Dependencies:

(TE4)	TA2P1-13	(TE5)	TA2P1-14	(TE9)	TA2P1-20
(TE10)	TA2P1-23	(TE26)	TA2P1-7	(TE30)	TP2-A2
(CP9)	A2C8	(CP12)	A2CR10	(CP22)	A2CR9
(CP28)	A2Q6	(CP29)	A2Q7	(CP30)	A2Q8
(CP40)	A2R18	(CP41)	A2R19	(CP43)	A2R20
(CP44)	A2R21	(CP46)	A2R23	(CP47)	A2R24
(CP49)	A2R26	(CP50)	A2R27	(CP51)	A2R28
(CP52)	A2R29	(CP54)	A2R30	(CP55)	A2R31
(CP66)	A2U1A	(CP68)	GNDA		

Test 33 Label = (TE33) TXA2P1-11
Dependencies:

Test 34 Label = (TE34) TXA2P1-13
Dependencies:

Test 35 Label = (TE35) TXA2P1-23
Dependencies:

Test 36 Label = (TE36) TXA2P1-14
Dependencies:

(TE33)	TXA2P1-11	(TE35)	TXA2P1-23	(CP70)	GNDD

Test 37 Label = (TE37) TXA2P1-7
Dependencies:

Test 38 Label = (TE38) TYA2P1-20
Dependencies:

Test 39 Label = (TE39) TXA2P1-8
Dependencies:

(TE33)	TXA2P1-11	(TE34)	TXA2P1-13	(TE35)	TXA2P1-23
(TE36)	TXA2P1-14	(TE37)	TXA2P1-7	(CP9)	A2C8
(CP40)	A2R18	(CP41)	A2R19	(CP43)	A2R20
(CP44)	A2R21	(CP45)	A2R22	(CP66)	A2U1A
(CP68)	GNDA	(CP70)	GNDD	(CP101)	A2C8S
(CP102)	A2U1-2				

Test 40 Label = (TE40) TXP3-A2
Dependencies:

(TE38)	TYA2P1-20	(TE49)	TPA-A2	(CP48)	A2R25
(CP49)	A2R26				

Test 41 Label = (TE41) TXP4-A2
Dependencies:

(TE35)	TXA2P1-23	(TE38)	TYA2P1-20	(TE49)	TPA-A2
(CP3)	A2C11	(CP12)	A2CR10	(CP22)	A2CR9
(CP29)	A2Q7	(CP30)	A2Q8	(CP49)	A2R26
(CP50)	A2R27	(CP51)	A2R28	(CP52)	A2R29

(CP54) A2R30 (CP55) A2R31 (CP57) A2R33

(C

P58) A2R34 (CP68) GNDA (CP70) GNDD

Test 42 Label = (TE42) TYA2P1-17
Dependencies:
(TE35) TXA2P1-23 (TE38) TYA2P1-20 (TE49) TPA-A2
(CP3) A2C11 (CP12) A2CR10 (CP13) A2CR11
(CP14) A2CR12 (CP22) A2CR9 (CP29) A2Q7
(CP30) A2Q8 (CP49) A2R26 (CP50) A2R27
(CP51) A2R28 (CP52) A2R29 (CP54) A2R30
(CP56) A2R32 (CP57) A2R33 (CP58) A2R34
(CP68) GNDA (CP70) GNDD

Test 43 Label = (TE43) TR16
Dependencies:
(CP96) A2R16 (CP102) A2U1-2

Test 45 Label = (TE45) TR17
Dependencies:
(CP82) A2C10 (CP94) A2R17 (CP98) A2U1-11
(CP101) A2C8S (CP102) A2U1-2 (CP105) A2CR12S

Test 47 Label = (TE47) TR33
Dependencies:
(CP3) A2C11 (CP57) A2R33 (CP58) A2R34

Test 48 Label = (TE48) TR35
Dependencies:
(CP92) A2R35 (CP93) A2C12

Test 49 Label = (TE49) TPA-A2
Dependencies:
(TE33) TXA2P1-11 (TE34) TXA2P1-13 (TE35) TXA2P1-23
(TE36) TXA2P1-14 (TE37) TXA2P1-7 (TE38) TYA2P1-20
(CP3) A2C11 (CP9) A2C8 (CP12) A2CR10
(CP22) A2CR9 (CP28) A2Q6 (CP29) A2Q7
(CP40) A2R18 (CP41) A2R19 (CP43) A2R20
(CP44) A2R21 (CP46) A2R23 (CP47) A2R24
(CP49) A2R26 (CP66) A2U1A (CP68) GNDA
(CP70) GNDD (CP101) A2C8S (CP102) A2U1-2
(CP105) A2CR12S

Test 50 Label = (TE50) TXA2P1-25
Dependencies:
(TE10) TA2P1-23 (CP68) GNDA (CP71) A2C7S
(CP72) A2C6S (CP73) A2CR8S

Test 51 Label = (TE51) TXA2P1-32
Dependencies:
(TE10) TA2P1-23 (CP8) A2C7 (CP21) A2CR8
(CP68) GNDA (CP71) A2C7S (CP72) A2C6S
(CP73) A2CR8S

Test 52 Label = (TE52) T+30STTO
Dependencies:
(CP6) A2C3

Test 53 Label = (TE53) T+15STTO

Dependencies:
(CP81) A2C9 (CP100) A2U1-4

Test 54 Label = (TE54) T-15STTO
Dependencies:
(CP82) A2C10 (CP98) A2U1-11

Test 55 Label = (TE55) TR14
Dependencies:
(CP86) A2U1-3 (CP95) A2R14

Test 56 Label = (TE56) TYA2P1-8
Dependencies:
(CP84) A2R15 (CP86) A2U1-3

End of dependency display

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

End of associated failure group display

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Weight Printed is Test Costs

Test 1	Label = TA2P1-1	Weight =	0.00
Test 2	Label = TA2P1-11	Weight =	0.00
Test 3	Label = TA2P1-12	Weight =	0.00
Test 4	Label = TA2P1-13	Weight =	0.00
Test 5	Label = TA2P1-14	Weight =	0.00
Test 6	Label = TA2P1-17	Weight =	0.00
Test 7	Label = TA2P1-19	Weight =	0.00
Test 8	Label = TA2P1-2	Weight =	0.00
Test 9	Label = TA2P1-20	Weight =	0.00
Test 10	Label = TA2P1-23	Weight =	0.00
Test 11	Label = TA2P1-24	Weight =	0.00
Test 12	Label = TA2P1-25	Weight =	0.00
Test 13	Label = TA2P1-26	Weight =	0.00
Test 14	Label = TA2P1-27	Weight =	0.00
Test 15	Label = TA2P1-29	Weight =	0.00
Test 16	Label = TA2P1-3	Weight =	0.00
Test 17	Label = TA2P1-30	Weight =	0.00
Test 18	Label = TA2P1-31	Weight =	0.00
Test 19	Label = TA2P1-32	Weight =	0.00
Test 20	Label = TA2P1-33	Weight =	0.00
Test 21	Label = TA2P1-34	Weight =	0.00
Test 22	Label = TA2P1-36	Weight =	0.00
Test 23	Label = TA2P1-37	Weight =	0.00
Test 24	Label = TA2P1-5	Weight =	0.00
Test 25	Label = TA2P1-6	Weight =	0.00
Test 26	Label = TA2P1-7	Weight =	0.00
Test 27	Label = TA2P1-8	Weight =	0.00
Test 28	Label = TA2P1-9	Weight =	0.00
Test 29	Label = TP1-A2	Weight =	0.00
Test 30	Label = TP2-A2	Weight =	0.00
Test 31	Label = TP3-A2	Weight =	0.00
Test 32	Label = TP4-A2	Weight =	0.00
Test 33	Label = TXA2P1-11	Weight =	0.00
Test 34	Label = TXA2P1-13	Weight =	0.00
Test 35	Label = TXA2P1-23	Weight =	0.00
Test 36	Label = TXA2P1-14	Weight =	0.00
Test 37	Label = TXA2P1-7	Weight =	0.00
Test 38	Label = TYA2P1-20	Weight =	0.00
Test 39	Label = TXA2P1-8	Weight =	0.00
Test 40	Label = TXP3-A2	Weight =	0.00
Test 41	Label = TXP4-A2	Weight =	0.00
Test 42	Label = TYA2P1-17	Weight =	0.00
Test 43	Label = TR16	Weight =	0.00
Test 45	Label = TR17	Weight =	0.00
Test 47	Label = TR33	Weight =	0.00
Test 48	Label = TR35	Weight =	0.00
Test 49	Label = TPA-A2	Weight =	0.00
Test 50	Label = TXA2P1-25	Weight =	0.00
Test 51	Label = TXA2P1-32	Weight =	0.00
Test 52	Label = T+30STTO	Weight =	0.00
Test 53	Label = T+15STTO	Weight =	0.00
Test 54	Label = T-15STTO	Weight =	0.00
Test 55	Label = TR14	Weight =	0.00
Test 56	Label = TYA2P1-8	Weight =	0.00

End of weight display. Weight= Test Costs

File Name: HVA2
File Description: HIGH VOLTAGE POWER SUPPLY A2 MODEL
File Date: 15SEPT89

Associated component group TEST RESISTORS

(CP31)	A2R1	(CP45)	A2R22	(CP48)	A2R25
(CP55)	A2R31	(CP62)	A2R6	(CP63)	A2R7
(CP65)	A2R9				

Associated component group FOCUS FB

(CP7)	A2C6	(CP20)	A2CR7

Associated component group +15KV OSC OUT2

(CP24)	A2Q2	(CP17)	A2CR4

Associated component group DYN FOCUS OUT

(CP56)	A2R32	(CP13)	A2CR11	(CP14)	A2CR12

Associated component group DYN FOCUS

(CP28)	A2Q6	(CP29)	A2Q7	(CP30)	A2Q8
(CP40)	A2R18	(CP41)	A2R19	(CP43)	A2R20
(CP44)	A2R21	(CP46)	A2R23	(CP47)	A2R24
(CP50)	A2R27	(CP51)	A2R28	(CP52)	A2R29
(CP54)	A2R30	(CP57)	A2R33	(CP58)	A2R34
(CP66)	A2U1A	(CP3)	A2C11	(CP22)	A2CR9
(CP9)	A2C8	(CP12)	A2CR10		

Associated component group FOCUS OSC IN

(CP64)	A2R8	(CP67)	A2VR1	(CP19)	A2CR6

Associated component group FOCUS OSC BIAS

(CP32)	A2R10	(CP33)	A2R11	(CP34)	A2R12
(CP35)	A2R13				

Associated component group +15KV OSC OUT1

(CP23)	A2Q1	(CP11)	A2CR1

Associated component group +15KV OSC BIAS

(CP42)	A2R2	(CP53)	A2R3	(CP60)	A2R4
(CP61)	A2R5	(CP1)	A2C1	(CP5)	A2C2
(CP15)	A2CR2	(CP16)	A2CR3		

Associated component group GROUNDS

(CP68)	GNDA	(CP69)	GNDC	(CP70)	GNDD

End of associated component group display